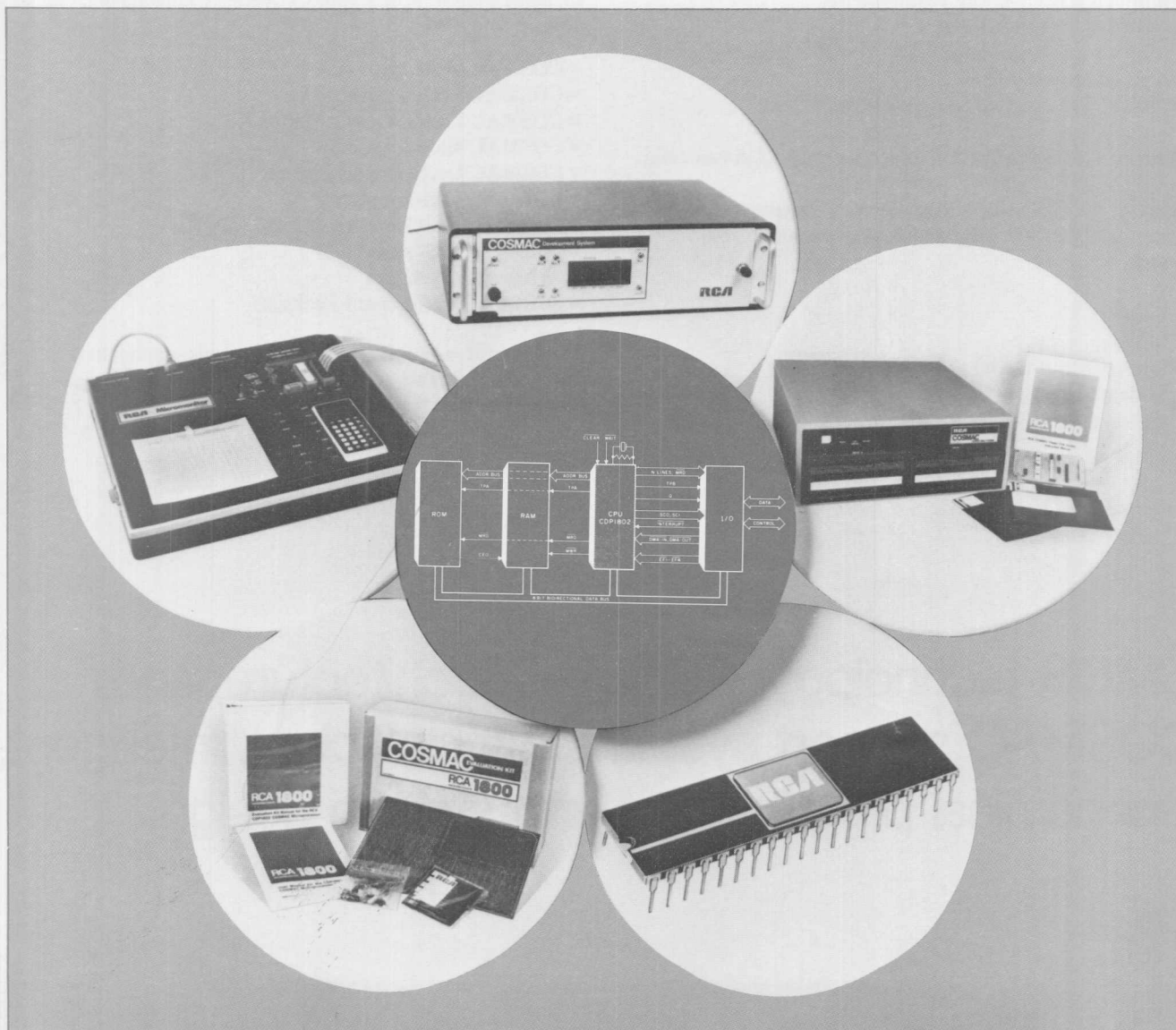


COMPONENTS DIVISION
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RCA Solid State

COSMAC Microprocessor Product Guide



MPG-180B

The RCA1800 microprocessor family includes all the elements you need to build an efficient microprocessor system.

Integrated Circuits (CDP1800 Series)

Our IC family boasts two important features: First, it's an all-CMOS family designed and manufactured by the First Family in CMOS. You get all the advantages of a CMOS system . . .

- minimal power-supply requirements
- completely static circuitry
- wide temperature range (-55 to +125°C) capability
- high noise immunity
- CMOS, TTL, NMOS compatibility . . .

plus the CMOS production expertise only RCA can offer.

Second, the CDP1800 series is comprehensive. It has a wide variety of ICs from which you can build your system . . .

- RAMs
- ROMs
- Input/Output (I/Os)
- System expanders

Support Systems (CDP18S Series)

RCA's theme in developing its hardware and software has been "Graduated Steps to Microprocessing". In both functions and dollar investment, we offer discrete, logical steps for you to follow. Our approach is to help you progress from a learning state right on through to integral hardware/software system prototyping, covering each step with an appropriate tool . . .

- COSMAC Microtutor II
- COSMAC Evaluation Kit
- COSMAC EK/Assembler-Editor Kit
- COSMAC Microterminal
- COSMAC Development System II
- COSMAC Micromonitor
- Micromonitor Operating System (MOPS)
- Floppy Disk System
- Arithmetic Packages
- Software Development Packages

All along the way, you'll use our manuals, application notes, and seminars to continually update your understanding of COSMAC.

CMOS technology, COSMAC architecture, and COSMAC support systems offer efficient, intelligent, economical programming and system design.

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1800 Family IC's and Support Systems

Microprocessors

CPU

CDP1802	COSMAC	5
CDP1804	COSMAC	12

ROM's (custom)

CDP1831	512 x 8	14
CDP1832	512 x 8	14
CDP1833	1024 x 8	14
CDP1834	1024 x 8	14

ROM's (standard)

CDPR512	UT4 Utility Program	15
CDPR522	Microterminal Controller	15
CDPR582	Fixed-Point Arithmetic	15

RAM's

CDP1821	1024 x 1	16
CDP1822	256 x 4	17
CDP1823	128 x 8	16
CDP1824	32 x 8	17
CDP1825	1024 x 4	18

General-Purpose Memories

MWS5101	256 x 4	31
MWS5114	1024 x 4	31
CD4036A	4 x 8	32
CD4039A	4 x 8	32
CD4061A	256 x 1	32
CD40061A	256 x 1	32
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Characteristic	Limits				Units
	Non-"C" Types		"C" Types		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Input-Voltage Range	V _{SS}	V _{DD}	V _{SS}	V _{DD}	

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(All voltage values referenced to V_{SS} terminal)

NON-"C" TYPES -0.5 to +11 V

"C" TYPES -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

OPERATING-TEMPERATURE RANGE (T_A):

CERAMIC PACKAGES (D SUFFIX TYPES) -55 to +125°C

PLASTIC PACKAGES (E SUFFIX TYPES) -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. +265°C

The CDP1802 microprocessor is an 8-bit silicon-gate CMOS device for use as a general-purpose computing or control element.

Features:

- 8-bit parallel bidirectional data bus
- 16-x-16-bit matrix of registers for easy programming
- DC to 6.4-MHz clock (single phase)
- Fast 2.5- or 3.75- μ s instruction time
- 91 basic instructions, 255 operation codes
- Minimal power-supply requirements — low current drain, single-supply, wide voltage range
- Split-power-supply option that allows for 10 V on internal parts of CPU and 5 V on interfacing lines
- Optional on-chip crystal-controlled oscillator
- Memory addressing to 65K bytes
- Adaptability to any combination of standard RAM, ROM, or PROM memories
- Maskable interrupt and 4 testable external flag lines
- On-chip DMA controls
- Simple RESET, LOAD, PAUSE, and RUN controls
- Programmable serial output (Q)

CDP1800 Series ICs are available in two performance selections:

A type without a "C" suffix is the high-performance device. For example, the CDP1802 has:

- 4 V to 10.5 V operating voltage range
- 2.5- or 3.75- μ s instruction time
- 100-mW power dissipation (typical conditions)
- 6.4-MHz maximum clock input frequency at 10 V.

A type with a "C" suffix, for example, the CDP1802C has:

- 4 V to 6.5 V recommended operating voltage range
- 5- or 7.5- μ s instruction time
- 10-mW power dissipation (typical conditions)
- 3.2-MHz maximum clock input frequency at 5 V

The Unique COSMAC Architecture

The COSMAC architecture is shown at the top of the facing page. The principal feature of this system is a register matrix consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated or selected by the 4-bit binary code from one of the designators P, X, or N. The contents of any register can be directed to any one of the following three paths:

1. to the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. to the accumulator (either of the two bytes can be gated to it);
3. to the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

How It Works

The registers in R can be used by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters — Any register can be used as the main program counter; the number of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction, the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the interrupt servicing routine, and at startup R(0) is the program counter. At other times, the register designated as program counter is at the discretion of the user.

Data Pointers — The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see the Instruction Summary on pages 46-47):

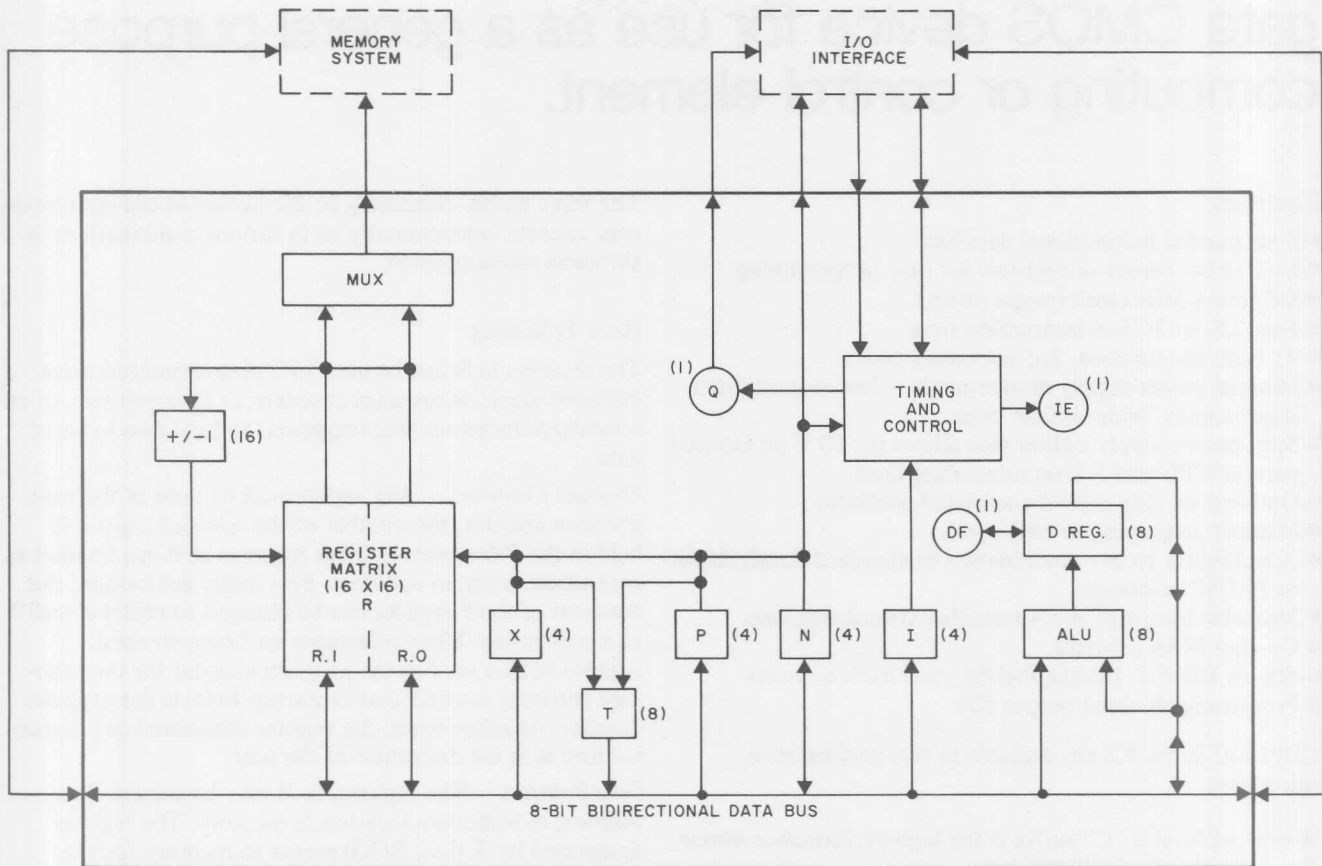
1. ALU operations F1-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions (F8-FD, FF, 7C, 7D, 7F). During these instruction executions, the operation is referred to as "data immediate."

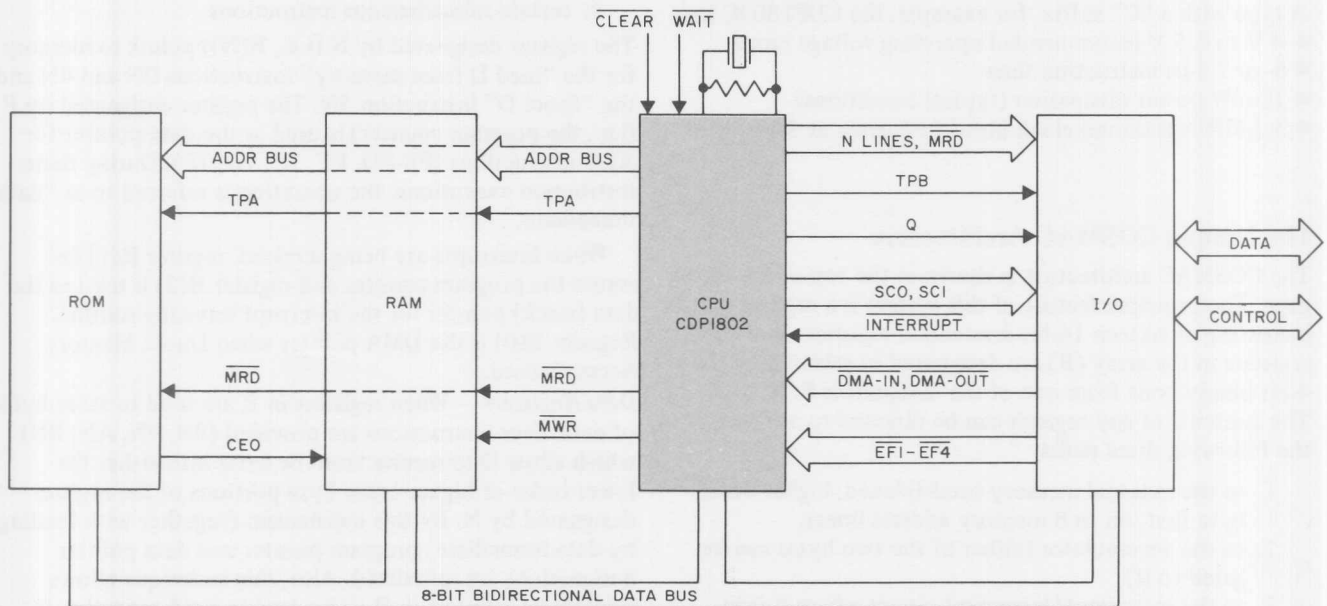
When interrupts are being serviced, register R(1) becomes the program counter and register R(2) is used as the data (stack) pointer for the interrupt servicing routine. Register R(0) is the DMA pointer when Direct Memory Access is used.

Data Registers — When registers in R are used to store bytes of data, four instructions are provided (8N, 9N, AN, BN) which allow D to receive from or write into either the lower-order or higher-order byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

CDP1802 COSMAC architecture



Typical CDP1802-based microcomputer system



DMA —Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-in or DMA-out request is received, the current instruction cycle is completed before the request is serviced. Upon entering the DMA state, the contents of R(O) is sent to memory as the address where the data is written into (DMA-in) or read from (DMA-out). At the completion of each DMA cycle, which is one machine cycle, the content of R(O) is incremented by 1 so that it points to the next memory location. Thus, R(O) is a dedicated DMA data pointer; if the DMA feature is not used, R(O) is available for any other function. (Since the CDP 1802 is a static machine and no refreshing is needed, there is no maximum number of DMA cycles that can be done consecutively.) This feature in the COSMAC architecture saves a substantial amount of logic when fast exchange of blocks of data are required, such as with magnetic disks or during CRT-display-refresh cycles.

Load Mode — A program load facility, using the DMA-in channel, is provided to enable users to load programs into memory. This facility provides a simple, one-step means for initially entering programs into the microprocessor system and eliminates the requirement for a specialized "bootstrap" program loader.

Interrupt Servicing — Register R(1) is always used as the program counter when interrupt servicing is initiated. When an interrupt request comes in and interrupts have been enabled (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values: 2 in X and 1 in P. Interrupt enable is automatically deactivated to inhibit further interruptions. The user written interrupt routine is now in control. The contents of T can be saved by means of a single instruction (78) in the memory location pointed to by R(X). At the conclusion of the interrupt, the return routine restores the pre-interrupted values of X and P with a single instruction (70 or 71). The interrupt-enable flip-flop can be enabled to permit further interrupts or can be disabled to prevent them.

Accumulator — The D register is an 8-bit accumulator. Connected directly to the ALU, the D register provides one operand for any arithmetic or logic function. The second operand is found in memory. Results from the ALU's operation are then stored back into D, appropriately setting the 1-bit data flag register (DF). A series of branch, shift, and arithmetical instructions are provided for operations based on either the value of D or DF.

The Q Flip-Flop — An internal flip-flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a bit serial output line.

Instruction Cycles

Most COSMAC instructions consist of two machine cycles, a fetch cycle and an execute cycle (a few instructions require two execute cycles). Each machine cycle is 8 clock

pulses long. During the fetch cycle, the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by 1 so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;
2. select an input or output port for data transfer;
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, etc.,
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

Conversing with the CDP1802: Signal Descriptions

BUS 0 to BUS 7 (Data Bus)

8-bit bidirectional DATA BUS lines. These lines are used for transferring data among the memory, the micro-processor, and the I/O devices.

TPA, TPB (2 Timing Pulses)

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

SC0, SC1 (2 State Code Lines)

These lines indicate that the CPU is: (1) fetching an instruction, or (2) executing an instruction, or (3) processing a DMA request, or (4) acknowledging an interrupt request. All states are valid at TPA.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

HIGH = V_{CC}
LOW = V_{SS}

MWR (Write Pulse)

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

MRD (Read Level)

A low level (V_{SS}) on MRD indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does not have a three-state high-impedance output, MRD is useful for driving memory bus separators. It is also used to indicate the direction of data transfer during an I/O instruction:

MRD= V_{CC} : Data from I/O to CPU and Memory

MRD= V_{SS} : Data from Memory to I/O or CPU

MA0 to MA7 (8 Memory Address Lines)

The higher-order byte of a 16-bit COSMAC memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system are strobed into external address latches by timing pulse TPA. (The CDP1831 and CDP1833 ROM's have built-in-address latches as well as other system-simplifying features, as listed on page 13.) The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 65K bytes.

N0, N1, N2 (I/O Selection)

These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding three lower order bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 and is indicated by the level of the MRD signal.

INTERRUPT, DMA-IN, DMA-OUT (3 I/O Requests)

These inputs are sampled by the CDP1802 during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit) requiring one machine cycle; and instruction execution is resumed by fetching the next instruction from M(R(1)).

DMA Action: Finish executing current instruction; R(O) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(O).

Note: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority, followed by DMA-OUT and then INTERRUPT.

EF1 to EF4 (4 Flags)

These inputs enable the I/O controllers to transfer status information to the processor. The lines can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which

case the program must routinely test the status of these flags. The flags are sampled at the beginning of every S1 cycle.

Q Flip-Flop

Single-bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK

Input for externally generated single-phase clock. The maximum clock frequency is 6.4 MHz at $V_{CC} = V_{DD} = 10$ volts. The clock is counted down internally to 8 clock pulses per machine cycle.

XTAL

Connection to be used with clock input terminal for an external crystal if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and XTAL) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be used for precise frequency adjustments.

WAIT, CLEAR (2 Control Lines)

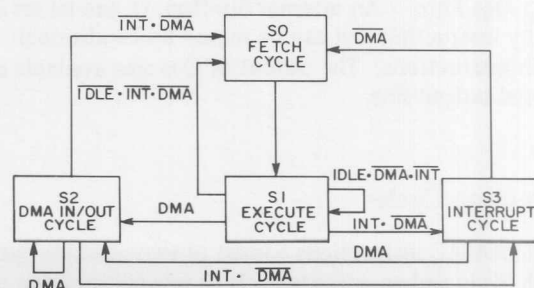
Provide four control modes as listed in the following truth table:

<u>CLEAR</u>	<u>WAIT</u>	MODE
H	H	RUN
H	L	PAUSE
L	H	RESET
L	L	LOAD

The functions of the modes are defined as follows:

Run — May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA(S2) cycle or fetch (S0) from location 0000 in memory.

The CDP1802 state transitions when in the RUN mode are shown below. Each machine cycle requires the same period of time — 8 clock pulses. The execution of an instruction pulse requires either two or three machine cycle, S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response.

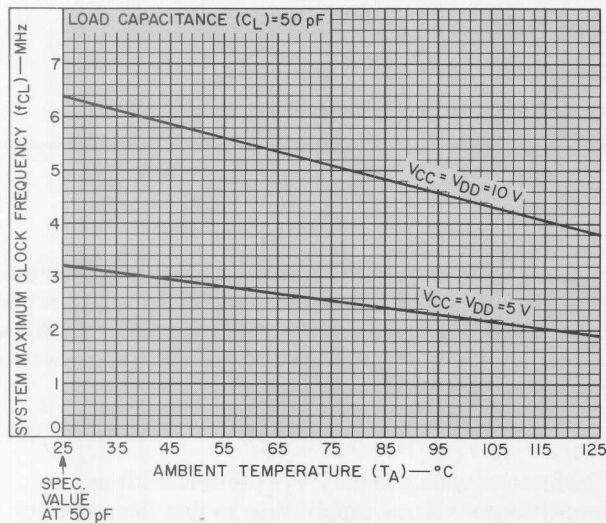


OPERATING CONDITIONS

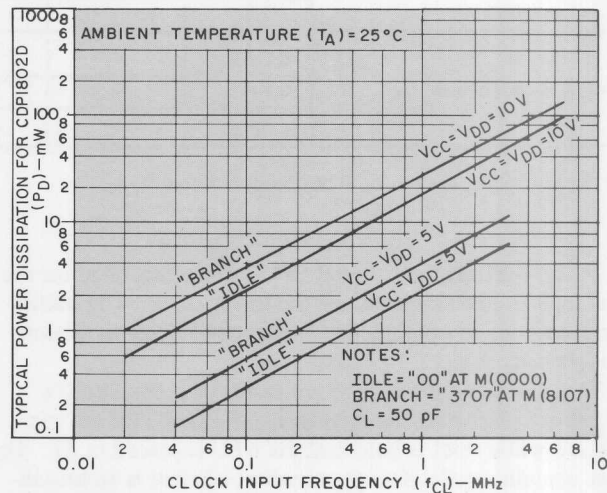
CHARACTERISTIC	CONDITIONS		VALUES AT 25°C		UNITS
	V _{CC} ¹ (V)	V _{DD} (V)	CDP1802	CDP1802C	
Supply-Voltage Range	—	—	4 to 10.5	4 to 6.5	V
Input Voltage Range	—	—	V _{SS} to V _{CC}	V _{SS} to V _{CC}	V
Maximum Clock Input Rise or Fall Time, t _r or t _f	—	—	1	1	μs
Instruction Time ²	5	5	5	5	μs
	5	10	4	—	
	10	10	2.5	—	
Maximum DMA Transfer Rate	5	5	400	400	KBytes/sec
	5	10	500	—	
	10	10	800	—	
Maximum Clock Input Frequency, f _{CL} ³	5	5	DC — 3.2	DC — 3.2	MHz
	5	10	DC — 4	—	
	10	10	DC — 6.4	—	

NOTES:

1. V_{CC} ≤ V_{DD}; for CDP1802C V_{CC} = V_{DD} = 5 volts.
2. Equals 2 machine cycles—one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles—one Fetch and two Execute operations.
3. Load Capacitance (C_L) = 50 pF.



Typical maximum clock frequency as a function of temperature.



Typical power dissipation as a function of clock frequency for BRANCH instruction and IDLE instruction for CDP1802.

STATIC ELECTRICAL CHARACTERISTICS

At $T_A = -40$ to $+85^\circ\text{C}$ and $V_{DD} = \pm 5\%$, except as noted.

5-Volt data apply to both the CDP1802D and the CDP1802CD. 10-Volt data apply to the CDP1802D only.

CHARACTERISTIC	CONDITIONS			LIMITS			UNITS
	V_O (V)	V_{IN} (V)	$V_{CC},$ V_{DD} (V)	Min.	Typ.*	Max.	
Quiescent Device Current, I_L : CDP1802 CDP1802C	—	—	5	—	1	100	μA
	—	—	10	—	10	500	
	—	—	5	—	10	500	
	—	—	10	—	—	—	
Output Low Drive (Sink) Current, I_{OL} (Except XTAL)	0.4	0.5	5	1.89	2.2	—	mA
	0.5	0.10	10	3.53	5.2	—	
XTAL Output I_{OL}	0.4	5	5	126	—	—	μA
Output High Drive (Source Current) I_{OH} (Except XTAL)	4.6	0.5	5	-0.44	-0.51	—	mA
	9.5	0.10	10	-1.07	-1.3	—	
XTAL Output I_{OH}	4.6	0	5	-63	—	—	μA
Output Voltage Low-Level V_{OL}	—	0.5	5	—	0	0.00	V
	—	0.10	10	—	0	0.05	
Output Voltage High Level, V_{OH}	—	0.5	5	4.95	5	—	
	—	0.10	10	9.95	10	—	
Input Low Voltage V_{IL}	0.5, 4.5	—	5	—	—	1.5	V
	0.5, 4.5	—	5, 10	—	—	1	
	1.9	—	10	—	—	3	
Input High Voltage V_{IH}	0.5, 4.5	—	5	—	—	3.5	
	0.5, 4.5	—	5, 10	—	—	4	
	1.9	—	10	—	—	7	

*Typical Values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

Pause — Stops the internal CPU timing generator on the first high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

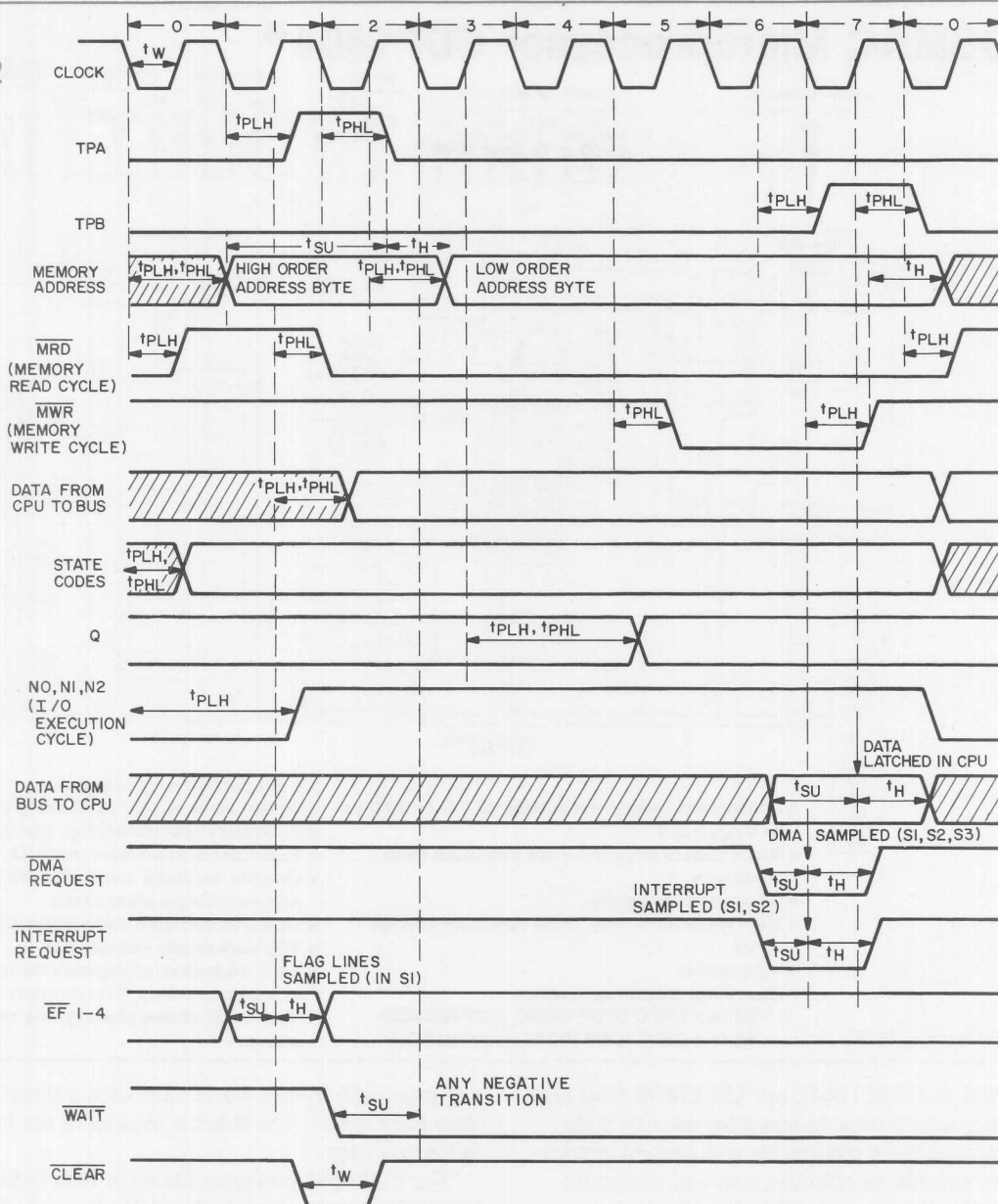
Reset — Registers I, N, Q are reset, IE is set, and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle. During this cycle the CPU remains in S1 and registers X, P, and R(O) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or S2. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE so as to preclude interrupts until ready for them. Power-up reset can be realized by connecting a buffered RC network to CLEAR.

Load — Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that the termination of the DMA-in operation does not force execution of the next instruction.

V_{DD} , V_{SS} , V_{CC} (Power Levels)

The internal voltage supply V_{DD} is isolated from the Input/Output voltage supply V_{CC} so that the processor may operate at high speed while interfacing with lower voltage elements such as TTL, NMOS, and LEDs. V_{CC} must be less than or equal to V_{DD} . All outputs swing from V_{SS} to V_{CC} . The recommended input voltage swing is V_{SS} to V_{CC} .

CDP1802 Timing Diagram



NOTES:

1. THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE
2. ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS
3. SHADED AREAS INDICATE "DON'T CARE" OR UNDEFINED STATE; MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD

CDP1802 INSTRUCTION EXECUTION TIMES

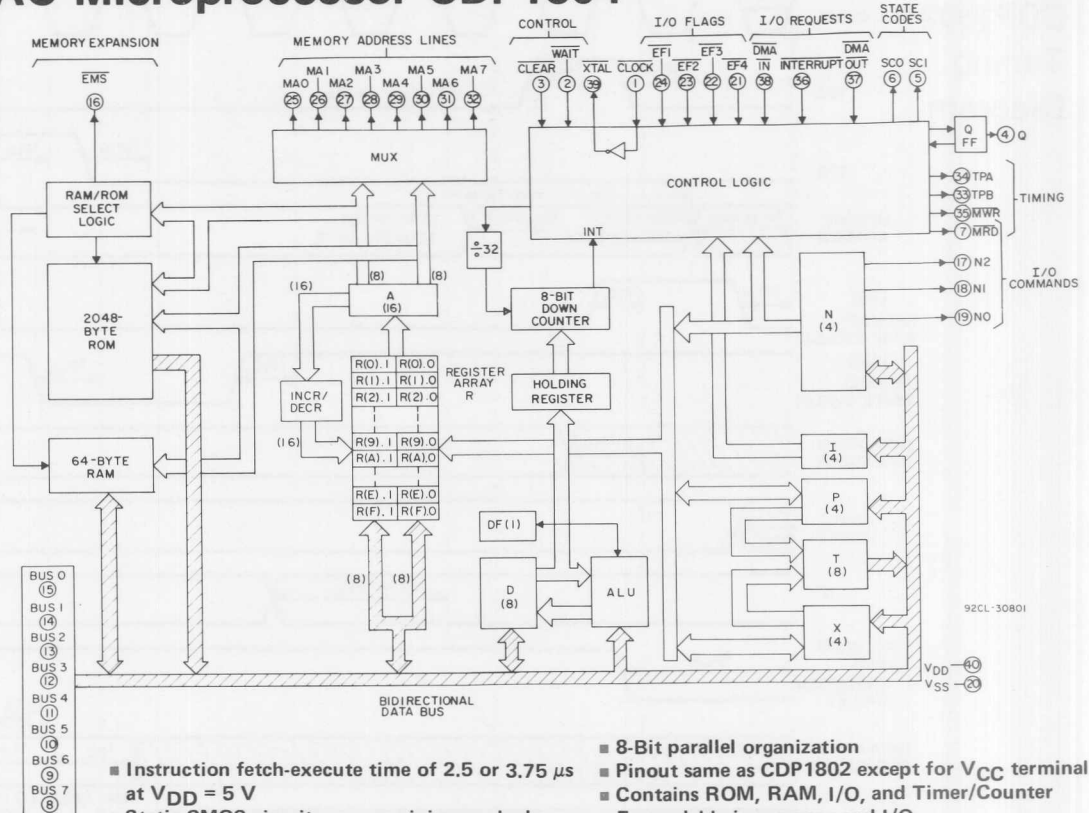
1-Byte instructions require 2 Machine Cycles: 1 Fetch, 1 Execute.

2-Byte instructions also require 2 Machine Cycles: 1 Fetch, 1 Execute.

3-Byte instructions require 3 Machine Cycles: 1 Fetch, 2 Executes.

INSTRUCTION SIZE			% OF TOTAL REPERTOIRE	INSTRUCTION TIME @ f =		
Bytes of Op. Code	Bytes of Address or Data	Total Bytes of Memory		6.4 MHz	3.2 MHz	2 MHz
1	0	1	93	2.5 μ s	5 μ s	8 μ s
1	1	2				
1	2	3	7	3.75 μ s	7.5 μ s	12 μ s
Average Instruction Execution Time			—	2.6 μ s	5.2 μ s	8.3 μ s

New COSMAC Microprocessor CDP1804*



- Instruction fetch-execute time of 2.5 or 3.75 μ s at $V_{DD} = 5$ V
- Static CMOS circuitry — no minimum clock frequency
- Single voltage supply
- High noise immunity, wide operating voltage range
- Low power
- Operating temperature range:
 - 55 to +125°C (CDP1804D, CDP1804CD)
 - 40 to +85°C (CDP1804E, CDP1804CE)

- 8-Bit parallel organization
- Pinout same as CDP1802 except for V_{CC} terminal
- Contains ROM, RAM, I/O, and Timer/Counter
- Expandable in memory and I/O
- On-chip oscillator controlled by crystal or RC network; single phase clock
- Upwards software compatible with CDP1802
- 106 easy-to-use instructions
- 16 $\times$ 16 matrix of registers for use as multiple program counters, data pointers or data registers
- Test mode allows prototyping with external memory

* Available second quarter 1979.

The CDP1804 and CDP1804C are LSI CMOS 8-bit register-oriented microcomputers designed for use in a wide variety of general-purpose computing and control applications. They can provide an effective cost and minimum chip count solution for many low-level applications.

The CDP1804 contains a 2048-bit mask-programmable ROM, 64 bytes of executable RAM, and an 8-bit presettable down-counter with a conditional $\div 32$ prescaler, in addition to the standard architecture of the CDP1802 microprocessor. This includes a bank of 16 registers of 16 bits each that can be used as multiple program counters, pointers to data in memory, or as data storage registers and a complement of Input/Output lines including 3 "N-bit" selection lines, four flag-input lines, 1 serial-output line and the DMA and Interrupt Request inputs.

Upwards software compatibility is maintained since the CDP1804 contains the entire instruction set of the CDP1802 plus added instructions for control of the counter. The terminal arrangements of the two devices are identical except that the V_{CC} terminal is eliminated, and an External Memory Select (EMS) terminal is substituted. This output is at low level whenever external memory is being addressed, allowing simple add-on external memory expansion. The starting address for the internal ROM is 0000; the starting address for the RAM is programmable in increments of

one page (256 bytes). RAM addresses will not wrap within their page space. The RAM is located in the lower 64 bytes of a page.

The CDP1804 performs the same functions as the CDP1802, except that the Load Mode of the CDP1802 is replaced with a Test Mode in the CDP1804. The Test Mode disables both internal ROM and RAM, and enables external memory. The new instructions for the counter are all 3-cycle instructions. Timing for the CDP1804 is the same as the CDP1802, except 4.5 clock pulses are provided for memory access and flag lines are sampled at the end of the S0 machine cycle.

The counter/timer generates an interrupt at count '0' and then is automatically reinitialized. It has several modes of operation, all under software control:

- Event counter - counter decremented by EF1 or EF2.
- Timer - counter decremented by TPA divided by 32.
- Pulse duration measurements - TPA clocks to counter are gated by EF1 or EF2 lines.

The CDP1804 and CDP1804C are functionally identical. They differ in that the CDP1804 has an operating voltage range of 4 to 10.5 volts and the CDP1804C has an operating voltage range of 4 to 6.5 volts. Both are supplied in 40-lead hermetic dual-in-line ceramic packages (D suffix) and in 40-lead dual-in-line plastic packages (E suffix).

Memory System Circuits for the CDP1802 include CMOS ROMs and RAMs with many system-simplifying capabilities

Features:

- Low power consumption
- All fully static parts
- Single power supply
- Direct interfacing with 1800-series microprocessor systems
- 3-state outputs
- TTL drive capability
- Industry standard pin-outs
- Different parts designed for small, medium, or large memory systems

Parts List:

ROMs (custom)

512 X 8	CDP1831
512 X 8	CDP1832*
1024 X 8	CDP1833
1024 X 8	CDP1834▲

*Pin-compatible with 2704

▲Pin-compatible with 2708

ROMs (standard)

Utility Program UT4	CDPR512
Microterminal	
Controller UT5	CDPR522
Fixed-Point Arithmetic	CDPR582

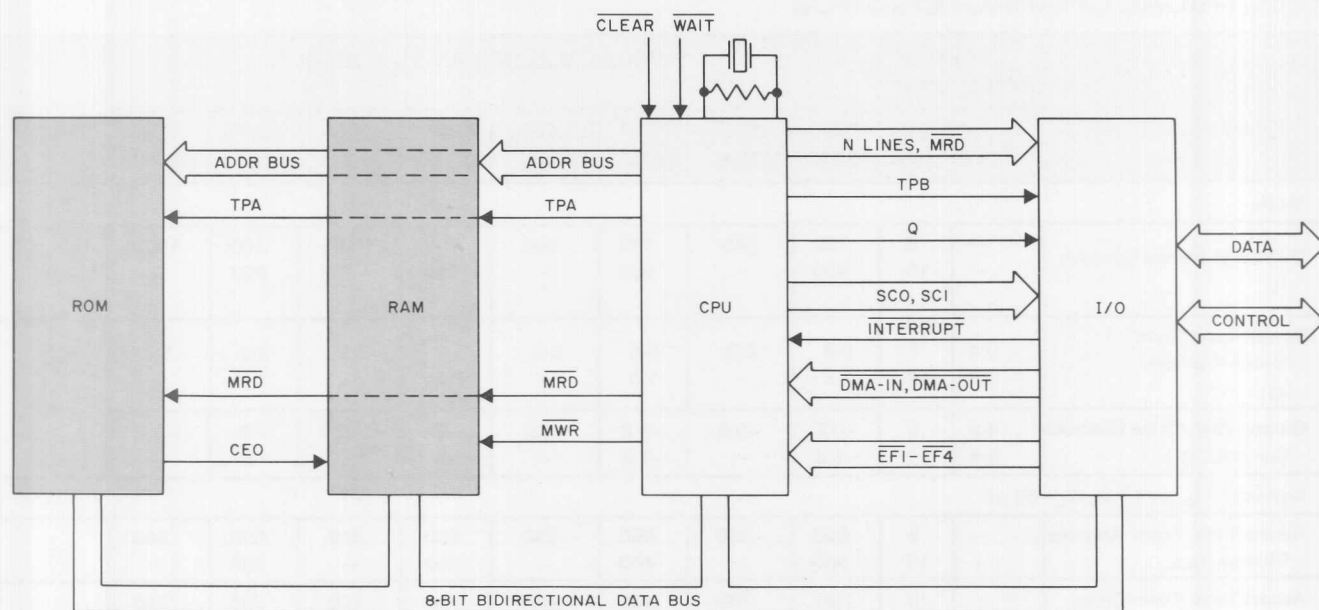
RAMs

1024 X 1	CDP1821
256 X 4	CDP1822
128 X 8	CDP1823
32 X 8	CDP1824
1024 X 4	CDP1825

System Expanders

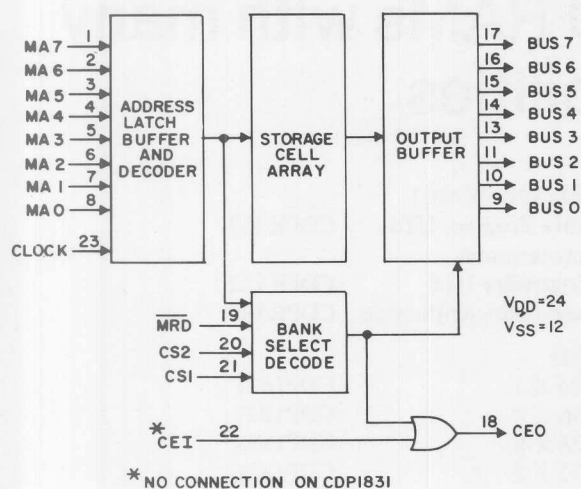
4-Bit Bus Buffer/ Separator	CDP1856
Memory Address Latch with Dual 1 of 4 Decoders	CDP1858
Memory Address Latch with 1 of 4 Decoder	CDP1859

Typical CDP1802-based microcomputer system



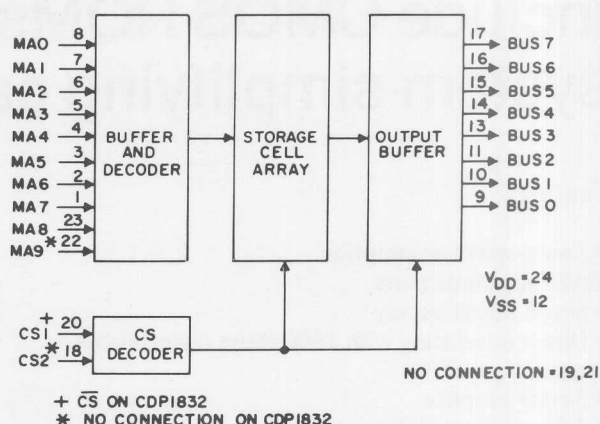
92CM-29727

512x8 ROM CDP1831



- User programs ROM's location in memory field
- Mask programmable
- On-chip latch for higher-order memory address
- CEO signal indicates status of chip (selected or not)
- Can minimize or eliminate memory decoding logic
- Either 512 or 1024 bytes of ROM in same pin-out
- 2 chip selects
- 3-state outputs
- Single power supply
- Industry standard 24-pin packages
- 400-ns access time at 10 V
- Directly compatible with CDP1802

512x8 ROM CDP1832



- CDP1832 is pin compatible with the 2704 PROM
- CDP1834 is pin compatible with the 2708 PROM
- Compatible with the CDP1802
- Mask programmable

1024x8 ROM CDP1834

- Single power supply
- 400-ns access time at 10 V
- 3-state outputs
- Industry standard 24-pin packages
- Accepts standard memory address decoding

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES AT T _A = 25°C								UNITS
	V _O (V)	V _{DD} (V)	CDP-1831	CDP-1831C	CDP-1832	CDP-1832C	CDP-1833	CDP-1833C	CDP-1834	CDP-1834C	
Static											
Quiescent Device Current, I _L	— —	5 10	100 500	500 —	100 500	500 —	100 500	1000 —	100 500	1000 —	μA
Output Low Drive (Sink) Current, I _{OL}	0.4 0.5	5 10	0.8 1.8	0.8 —	0.8 1.8	0.8 —	3.2 7.2	3.2 —	3.2 7.2	3.2 —	mA
Output High Drive (Source) Current, I _{OH}	4.6 9.5	5 10	−0.8 −1.8	−0.8 —	−0.8 −1.8	−0.8 —	−2 −5	−2 —	−2 −5	−3.2 —	
Dynamic: t _r , t _f = 10 ns, C _L = 50 pF											
Access Time From Address Change, t _{AA}	— —	5 10	850 350	850 —	850 400	850 —	850 350	850 —	850 350	850 —	ns
Access Time From Chip Select, t _{ACS}	— —	5 10	700 250	700 —	400 200	400 —	700 300	700 —	700 300	700 —	ns
Chip Enable Output Delay Time Address, t _{CA}	— —	5 10	500 200	500 —	— —	— —	400 200	400 —	— —	— —	ns

Utility Program UT4 ROM CDPR512

Mask-programmed CDP1832 512 x 8 ROM for use in the COSMAC Evaluation Kit (CDP18S020).

Includes routines for:

- ASCII-code conversion
- Memory read and write commands
- System initialization

Microterminal Controller UT5 ROM CDPR522

Mask-programmed CDP1832 512 x 8 ROM for use with the COSMAC Microterminal (CDP18S021).

Includes routines for:

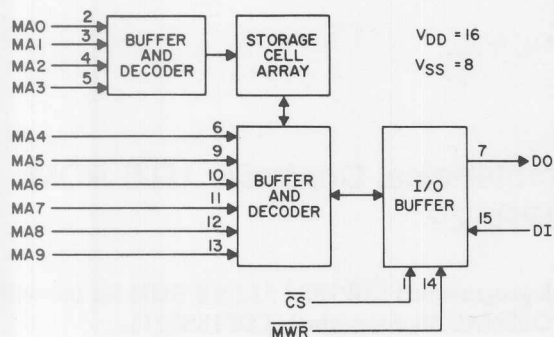
- Keyboard scan and debounce
- Digit, segment, and decimal point controls for a display
- Memory read and write commands
- System initialization

Fixed-Point Binary Arithmetic ROM CDPR582

Mask-programmed CDP1833 1024 x 8 ROM containing a fixed-point binary arithmetic subroutine package

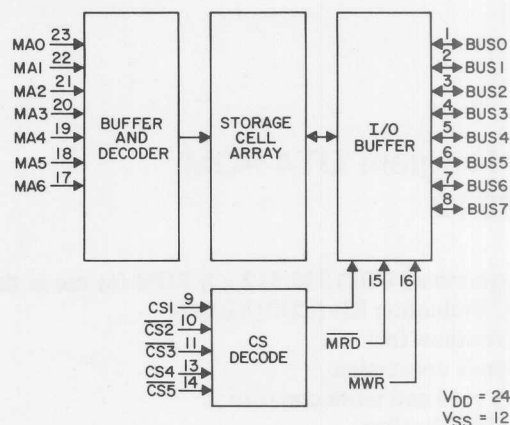
- Contains 15 arithmetic routines including:
 - 16-bit 2's-complement addition
 - 16-bit 2's complement subtraction
 - 16-bit 2's complement multiplication yielding 32-bit products
 - 32-bit 2's-complement division yielding 16-bit quotient and remainder
- Contains 14 utility subroutines and 2 format conversions (binary-to-BCD and BCD-to-binary)
- Programmed for starting address C000 (hex)
- Suitable for inclusion in any CDP1802-based system

1024x1 RAM CDP1821



- Interfaces with CDP1802 at full speed
- Good for large RAM memory systems
- Single power supply
- Industry standard 16-pin packages for high board density
- 200-ns access time at 10 V
- CS can be used as an additional address line – no clocking required
- Standby power consumption of 5 mW (typ.) at 10 V

128x8 RAM CDP1823

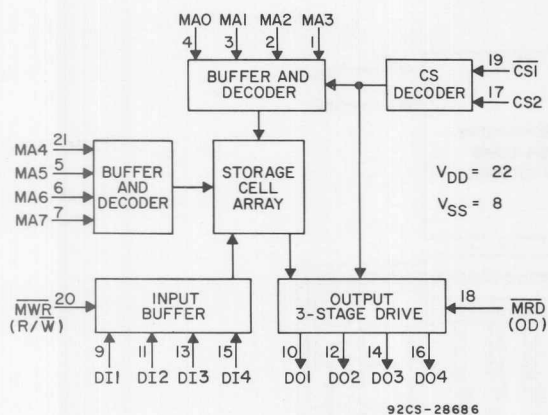


- 3-state bus
- Directly interfaces with CDP1802
- Standby power consumption of 5 mW (typ.) at 10 V
- Single power supply
- 200-ns access time at 10 V
- Industry standard 24-pin packages
- Designed for medium-sized RAM requirements

ELECTRICAL CHARACTERISTICS

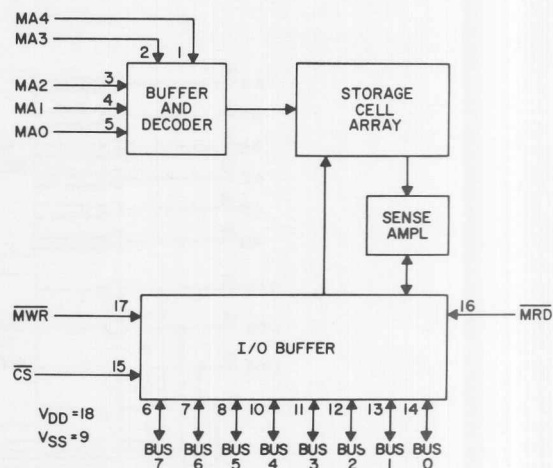
CHARACTERISTIC	TEST CONDITIONS			TYPICAL VALUES AT T _A = 25°C				UNITS
		V _O (V)	V _{DD} (V)	CDP- 1821	CDP- 1821C	CDP- 1823	CDP- 1823C	
Static								
Quiescent Device Current, I _L		— —	5 10	100 500	500 —	300 1000	1500 —	μA
Output Low Drive (Sink) Current I _{OL}	Any Output	0.4 0.5	5 10	2 3.5	2 —	1.2 1.8	1.2 —	mA
Output High Drive (Source) Current I _{OH}	Any Output	4.6 9.5	5 10	−1 −1.5	−1 —	−0.8 −1.8	−0.8 —	
Dynamic: t _r , t _f = 10 ns, C _L = 50 pF								
Read Operation								
Access Time From Address Change, t _{AA}		— —	5 10	350 200	350 —	350 200	350 —	ns
Access Time From Chip Select, t _{AC}		— —	5 10	250 150	250 —	250 150	250 —	ns
Total Power-Dissipation P _D at 1 μs cycle		— —	5 10	5 20	8 —	15 65	20 —	mW

256x4 RAM CDP1822



- Interfaces with CDP1802 at full speed
- 2 chip selects for easy memory expansion
- 150-ns (typ.) access time at 10 V
- Output disable permits common I/O systems
- Industry standard 22-pin packages
- Standby power consumption of 5 mW (typ.) at 10 V

32x8 RAM CDP1824

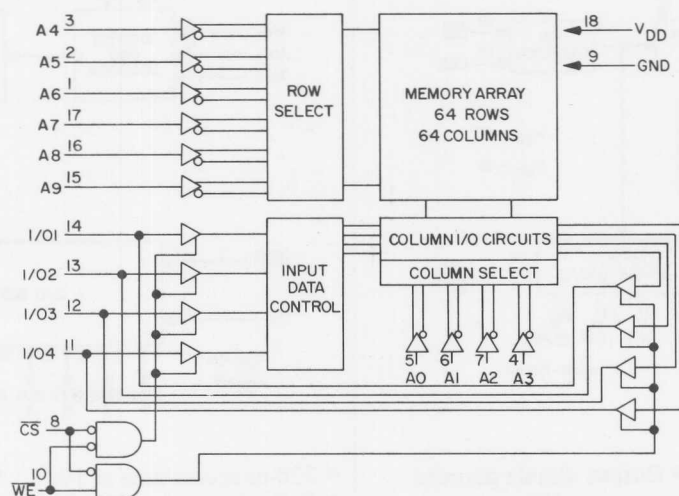


- 320-ns access time at 10 V
- Fully decoded and static
- Separate read and write signals
- Standby power consumption of 2.5 mW (typ.) at 10 V
- Low quiescent and operating power
- Excellent for minimum RAM systems (e.g., stacks)
- Industry standard 18-pin packages
- CS for memory expansion

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS		LIMIT VALUES AT T _A = -40 to +85° C, V _{DD} = ±5%				UNITS	
	V _O (V)	V _{DD} (V)	CDP-1822	CDP-1822C	CDP-1824	CDP-1824C		
Static								
Quiescent Device Current, I _L Max.		— —	5 10	500 1000	500 —	100 500	500 —	μA
Output Low Drive (Sink) Current I _{OL} Min.	Any Output	0.4 0.5	5 10	2 4.5	2 —	1.8 3.6	1.8 —	
Output High Drive (Source) Current I _{OH} Min.	Any Output	4.6 9.5	5 10	-1 -2.2	-1 —	-1.8 -3.6	-1.8 —	mA
Dynamic: t _r , t _f = 10 ns, C _L = 50 pF								
Read Operation								
Max. Access Time From Address Change, t _{AA}		— —	5 10	450 250	450 —	710 320	710 —	ns
Max. Access Time From Chip Select, t _{AC}		— —	5 10	450 250	450 —	710 320	710 —	ns

1024 x 4 RAM CDP1825



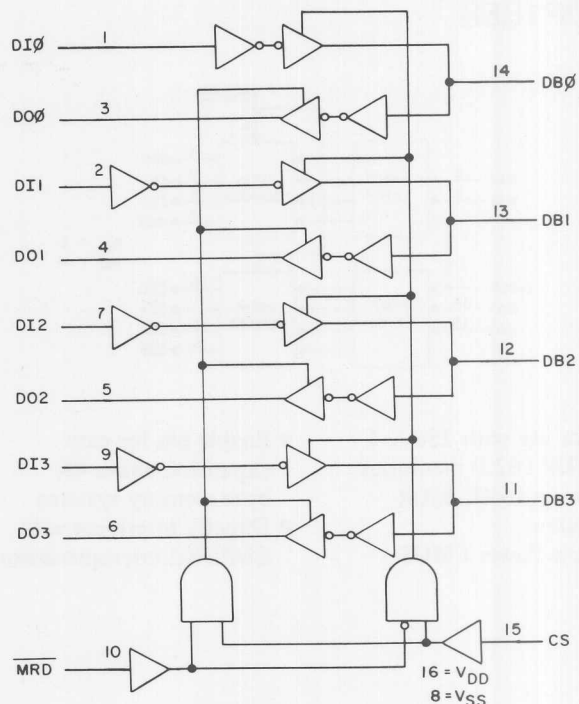
- Fully static operation
- 3-state outputs
- Industry-standard 18-pin package
- Single power-supply operation
- Common data input and output
- Memory retention for standby-battery voltage of 2 V min.
- All inputs and outputs are TTL compatible
- Low operating current

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	LIMIT VALUES AT T _A = -40 to +85°C, V _{DD} = ±5%						UNITS
		V _O (V)	V _{DD} (V)	CDP1825		CDP1825C		
				Min.	Max.	Min.	Max.	
Static								
Quiescent Device Current, I _L	$\overline{\text{CS}}$ = High	— —	5 10	— —	200 2000	— —	200 —	μA
Output Low Drive (Sink) Current I _{OL}	Any Output	0.4 0.5	5 10	2 3.5	— —	1.5 —	— —	mA
Output High Drive (Source) Current I _{OH}	Any Output	4.6 9.5	5 10	-0.4 -0.8	— —	-0.4 —	— —	
Dynamic: t _r , t _f = 10 ns, C _L = 50 pF								
Read Operation								
Access Time From Address Change, t _{AA}		— —	5 10	— —	650 350	— —	650 —	ns
Access Time From Chip Select, t _{AC}		— —	5 10	— —	200 100	— —	200 —	ns

4-Bit Bus Buffer/Separator CDP1856 (Memory)

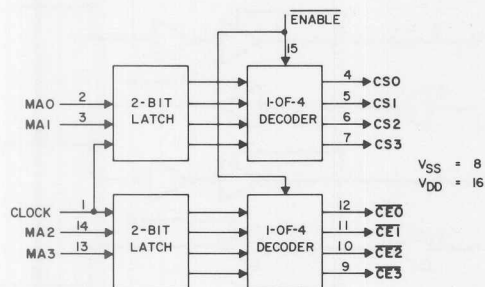
- Allows simple expansion of memory
- Connects directly to CPU's bidirectional data bus
- Non-inverting fully buffered data transfer
- Compatible with CDP1802 microprocessor at maximum speed
- CHIP SELECT input for simple system configurations
- Low quiescent and operating power



ELECTRICAL CHARACTERISTICS

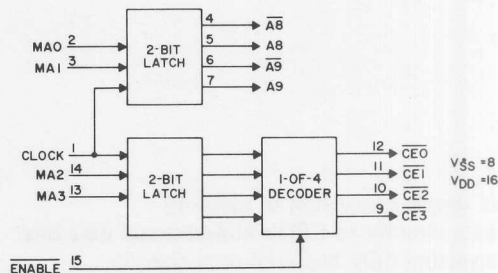
CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES AT T _A = 25° C		UNITS	
	V _O (V)	V _{DD} (V)	CDP-1856	CDP-1856C		
Static						
Quiescent Device Current, I _L		— — —	5 10	50 100	100 — —	μA
Output Low (Sink) Current, I _{OL}	Any Output	0.4 0.5	5 10	1.8 3.6	1.8 —	mA
Output High (Source) Current, I _{OH}	Any Output	4.6 9.5	5 10	−1.8 −3.6	−1.8 —	
Dynamic: t _r , t _f = 10 ns, C _L = 100 pF						
Propagation Delay Time: MRD or CS to DO, t _{ED}		— —	5 10	150 75	150 —	ns
MRD or CS to DB, t _{EB}		— —	5 10	150 75	150 —	ns
DI to DB, t _{IB}		— —	5 10	100 50	100 —	ns
DB to DO, t _{BD}		— —	5 10	100 50	100 —	ns

4-Bit Latch with Dual 1 of 4 Decoders CDP1858



- For use with 256 × 4 (CDP 1822) memories for up to 4K RAM system
- Low-Power CMOS
- Enable pin for easy expansion above 4K byte memory systems
- Directly interfaces with CDP1802 microprocessor

4-Bit Latch with 1 of 4 Decoder CDP1859



- Designed for use with 1024 × 1 (CDP1821) memories for up to 4K RAM system
- Low power CMOS
- Enable pin allows for easy expansion above 4K bytes of memory
- Directly interfaces with CDP1802 micro-processor

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS		TYPICAL VALUES AT T _A = 25°C					UNITS	
	V _O (V)	V _{DD} (V)	CDP- 1858	CDP- 1858C	CDP- 1859	CDP- 1859C			
Static									
Quiescent Device Current, I _L		— — —	5 10	50 100	100 — —	50 100	100 — —	μA	
	Output Low (Sink) Current, I _{OL}	0.4 0.5	5 10	1.6 3.6	1.6 —	1.6 3.6	1.6 —		mA
	Output High (Source) Current, I _{OH}	4.6 9.5	5 10	−1.6 −3.6	−1.6 —	−1.6 −3.6	−1.6 —		
Dynamic: t _r , t _f = 10 ns, I _L = 100 pF									
Propagation Delay Time: Clock L _H to Any Output	Enable=0	— —	5 10	220 110	220 110	220 110	220 110	ns	
		MA0, MA1 to CS0, CS1, CS2, or CS3	Clock=1 Enable=0	— —	5 10	200 90	200 90		— —
MA2, MA3 to $\overline{\text{CE0}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, or $\overline{\text{CE3}}$	Clock=1 Enable=0	— —	5 10	200 90	200 90	— —	— —	ns	
		MA0, MA1 to A8; A9, $\overline{\text{A8}}$ or $\overline{\text{A9}}$	Clock=X	— —	5 10	— —	— —		150 75
MA2, MA3 to $\overline{\text{CE0}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, or $\overline{\text{CE3}}$	Clock=1 Enable=0	— —	5 10	— —	— —	200 90	200 —	ns	
		X = DON'T CARE							

X = DON'T CARE

Input/Output System Circuits make use of many CDP1802 signals to lower cost and optimize performance.

Features:

- 4 CPU-tested flag inputs (EF lines) for binary inputs or for I/O-to-CPU signalling
- Interrupt request; maskable for flexibility
- 2 DMA request lines, in and out, with memory pointer and control logic on the CDP1802
- 2 state-code output lines to tell I/O devices what the CPU is doing
- Programmable output bit Q
- 3 I/O command lines (N) for programmed control of memory-I/O transfer
- Memory data strobe (TPB) for clean and easy capture of data by I/O device

Parts List:

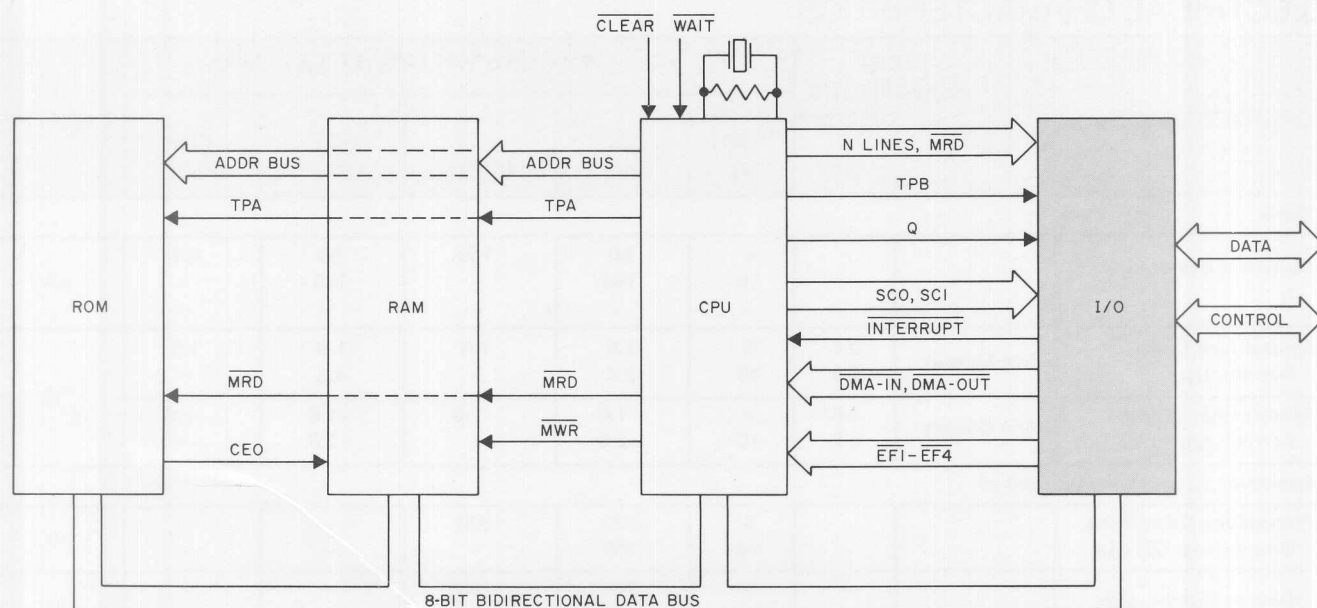
Programmable I/O Port
 Byte I/O Port
 N-Bit Decoder
 UART (Universal Asynchronous Receiver/Transmitter)
 Programmable Interface
 4-Bit Bus Buffer/Separator (I/O)
 Video Display Controller
 Color Generator
 Programmable Tone Generator
 PAL-Compatible TV Interface
 Latch and Decoder Memory Interface
 Latch and Decoder Memory Interface
 Latch and Decoder Memory Interface

CDP1851
 CDP1852
 CDP1853

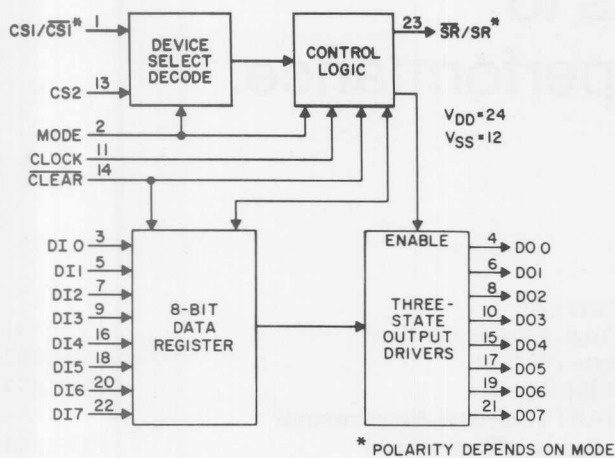
CDP1854
 CDP1855*
 CDP1857
 CDP1861
 CDP1862*
 CDP1863*
 CDP1864*
 CDP1866*
 CDP1867*
 CDP1868*

* Available fourth quarter 1978.

Typical CDP1802-based microcomputer system



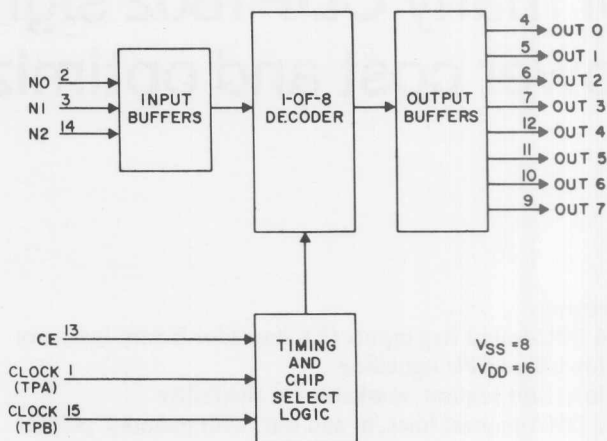
8-Bit Byte I/O Port
CDP1852



- 8-bit data latch
- Directly interfaces with CDP1802
- Industry standard 24-pin packages
- 3-state outputs
- Clear input
- Designed for use in 8-bit microprocessor systems
- Fully static
- Mode selectable

N-Bit Decoder

CDP1853



- Allows easy expansion of I/O systems
- Buffered inputs and outputs
- Functions at full microprocessor speed
- Ties directly to "N" lines on CDP1802
- Strobed outputs for spike-free decoding
- Low power dissipation
- Provides control of up to 14 I/O devices

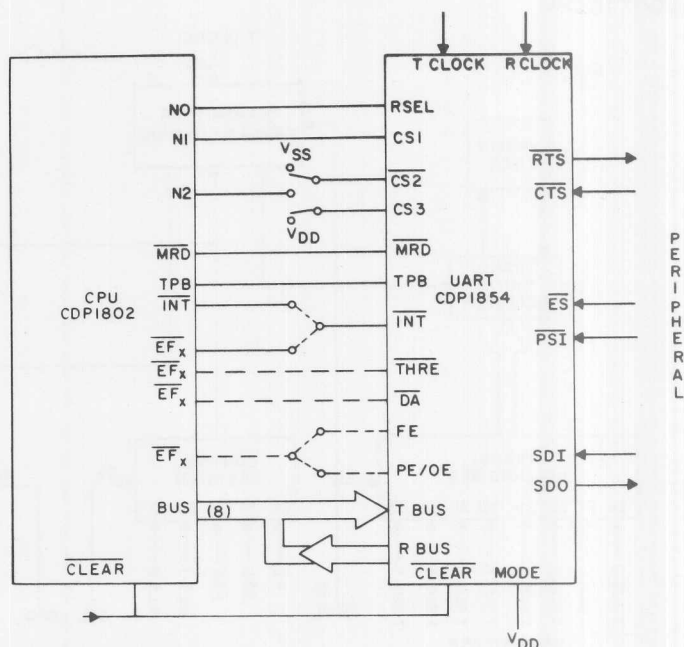
ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	TYPICAL VALUES AT $T_A = 25^\circ\text{C}$						UNITS
		V_O (V)	V_{DD} (V)	CDP-1852	CDP-1852C	CDP-1853	CDP-1853C	
Static								
Quiescent Device Current, I_L		— — —	5 10 —	50 100 —	100 — —	50 100 —	100 — —	μA
Output Low (Sink) Current, I_{OL}	Any Output	0.4 0.5	5 10	1.6 3.6	1.6 —	1.6 3.6	1.6 —	mA
Output High (Source) Current, I_{OH}	Any Output	4.6 9.5	5 10	—1.6 —3.6	—1.6 —	—1.6 —3.6	—1.6 —	
Dynamic: $t_r, t_f = 10\text{ ns}$, $C_L = 100\text{ pF}$								
Propagation Delay Time: Output from CS, t_{CA}		— —	5 10	200 100	200 —	— —	— —	ns
Data to Output, t_{OD}		— —	5 10	200 100	200 —	— —	— —	ns
CE to Output, t_{EOH} , t_{EOL}		— —	5 10	— —	— —	200 100	200 —	ns
N to Outputs, t_{NOH} , t_{NOL}		— —	5 10	— —	— —	250 120	250 —	ns

UART

CDP1854

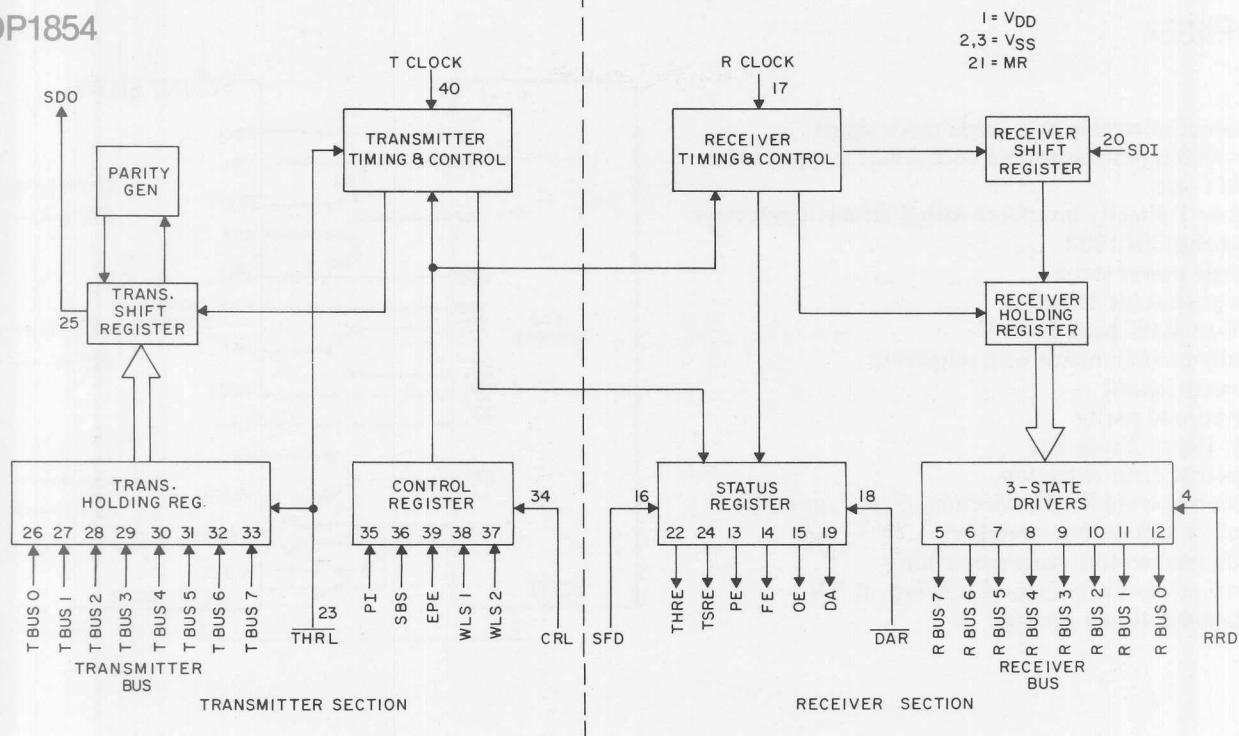
- Pin-out selectable by a single mode signal
- Mode 0 is pin-compatible with industry types 1602, 6011, etc.
- Mode 1 directly interfaces with 8-bit microprocessor like the CDP1802
- Single power supply
- False-start bit detection
- DC to 400K baud at 10 V
- Fully programmable with selectable:
 - parity inhibit
 - even/odd parity
 - 1, 1½, or 2 stop bits
- Overrun error detection
- External word length selection—5, 6, 7, or 8 bits
- Full or half duplex operation
- Full temperature range operation
- Low power dissipation—5 mW typ. at 5 V
- Standard 40-pin package



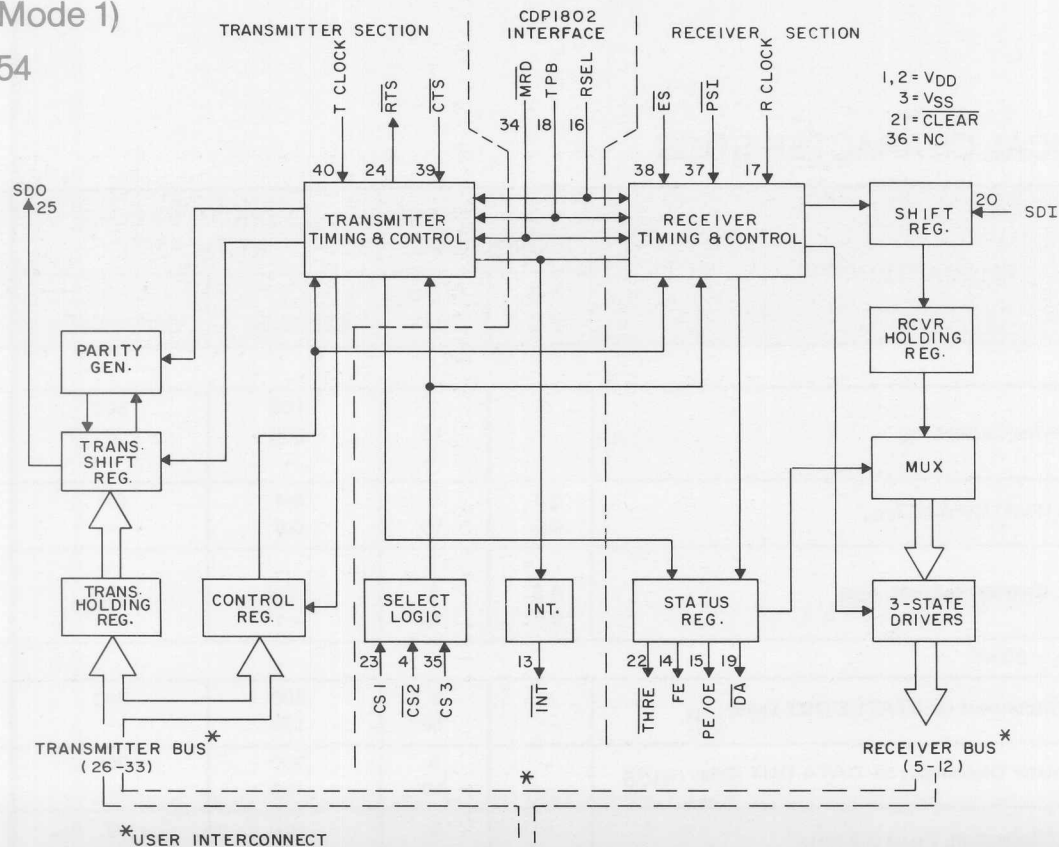
ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS		TYPICAL VALUES AT T _A = 25°C		UNITS
	V _O (V)	V _{DD} (V)	CDP1854	CDP1854C	
Static					
Quiescent Device Current, I _L	—	5	100	500	μA
	—	10	500	—	
	—	—	—	—	
Output Low (Sink) Current, I _{OL}	0.4	5	0.4	0.4	mA
	0.5	10	0.9	—	
Output High (Source) Current, I _{OH}	—	—	—	—	
	4.6	5	−0.4	−0.4	
	9.5	10	−1	—	
Dynamic, C _L = 50 pF					
Status Flag Disconnect to- STATUS OUT Delay, t _{ss}	—	5	200	200	ns
	—	10	100	—	
Receiver Register Disconnect to- DATA OUT Delay, t _{RDB}	—	5	200	200	ns
	—	10	100	—	
Total Power Dissipation, P _D at 3.2 MHz	—	5	5	7	mW
	—	10	15	—	

UART (Mode 0) CDP1854

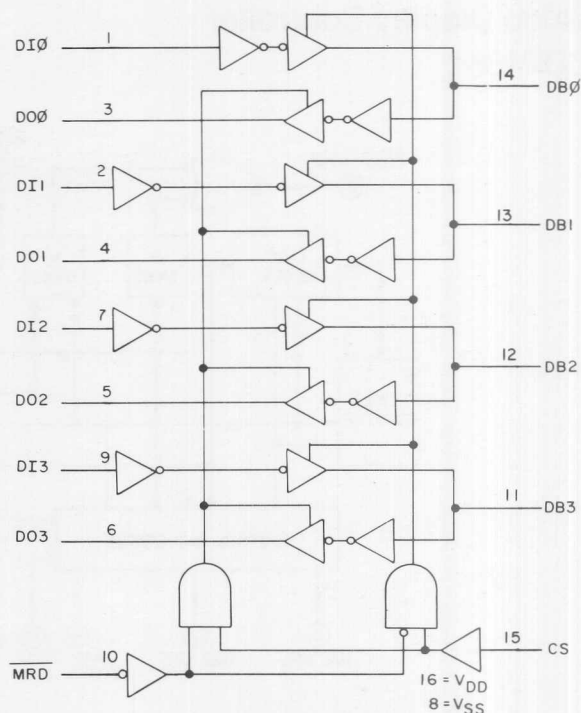


UART (Mode 1) CDP1854



4-Bit Bus Buffer/Separator CDP1857 (I/O)

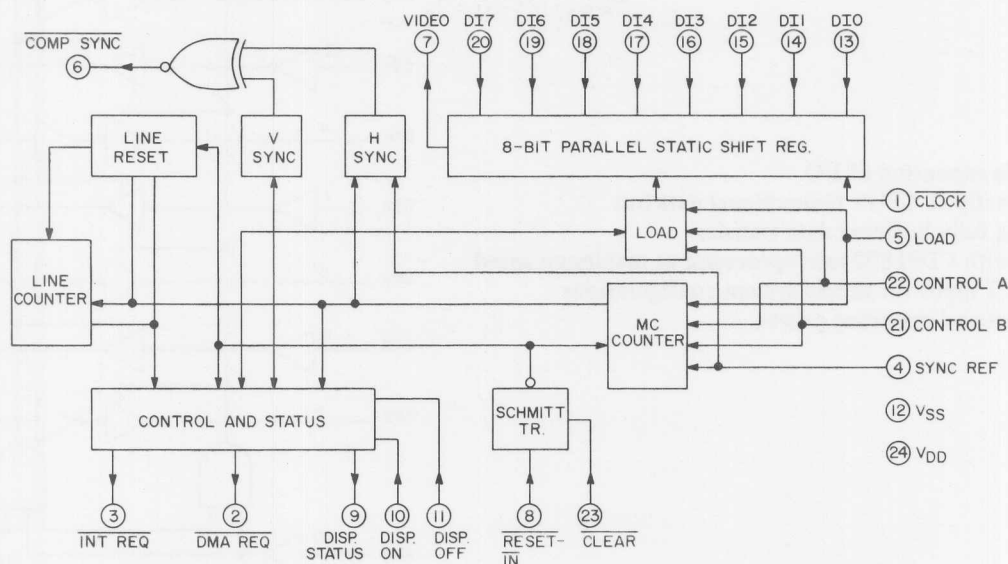
- Allows simple expansion of I/O
- Connects directly to CPU's bidirectional data bus
- Non-inverting fully buffered data transfer
- Compatible with CDP1802 microprocessor at maximum speed
- CHIP SELECT input for simple system configurations
- Low quiescent and operating power



ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES AT T _A = 25°C		UNITS	
	V _O (V)	V _{DD} (V)	CDP1857	CDP1857C		
Static						
Quiescent Device Current, I _L		— — —	5 10 —	50 100 —	100 — —	μA
Output Low (Sink) Current, I _{OL}	Any Output	0.4 0.5	5 10	1.8 3.6	1.8 —	mA
Output High (Source) Current, I _{OH}	Any Output	4.6 9.5	5 10	−1.6 −3.6	−1.6 —	
Dynamic: t _r , t _f = 10 ns, C _L = 100 pF						
Propagation Delay Time: MRD or CS to DO,, t _{ED}		— —	5 10	150 75	150 —	ns
MRD or CS to DB, t _{EB}		— —	5 10	150 75	150 —	ns
DI to DB, t _{IB}		— —	5 10	100 50	100 —	ns
DB to DO, t _{BD}		— —	5 10	100 50	100 —	ns

Video Display Controller CDP1861

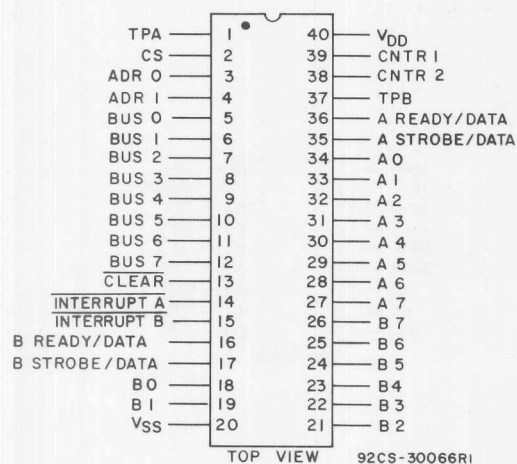


- Interfaces directly with CDP1802 microprocessor
- Supports bit-mapped video display for graphic flexibility
- Generates composite horizontal and vertical sync
- Programmable vertical resolution for matrix display of up to 64 x 128 segments
- Real-time interrupt generator
- Clear input
- External display control
- Designed to NTSC standards

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS		TYPICAL VALUES AT $T_A = 25^\circ\text{C}$	UNITS
	V_O (V)	V_{DD} (V)		
Quiescent Device Current, I_L	—	5	500	μA
Output Drive Current: Video or Sync	Output Low (Sink), I_{OL}	0.4	5	mA
	Output High (Source), I_{OH}	4.5	5	
Reset Out or Flag	Output Low (Sink), I_{OL}	0.4	5	mA
	Output High (Source), I_{OH}	4.5	5	
I/O Requests;	Output Low (Sink), I_{OL}	0.4	5	mA
Reset-In:	Positive Trigger Threshold, V_P	—	5	V
	Negative Trigger Threshold, V_N	—	5	V
Hysteresis Voltage, V_H	—	5	0.8	V

New Programmable I/O Interface CDP1851 *



- Silicon-gate CMOS circuitry
- Single voltage supply
- Operates in I/O or memory spaces
- 20 programmable I/O lines
- Programmable to operate in 1 of 4 modes

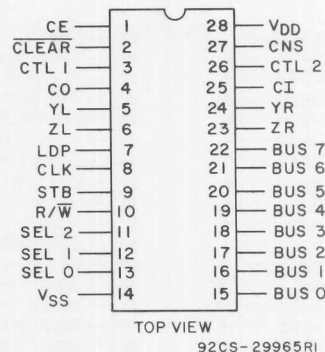
Input

Output

Bidirectional

Bit programmable * Available fourth quarter 1978.

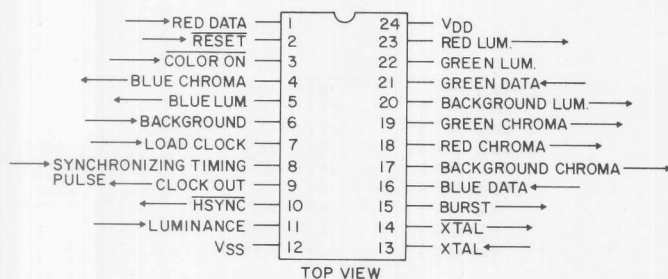
New Multiply-Divide Unit CDP1855 *



- Low-power static CMOS
- Performs binary multiplication or division under microprocessor control
- 8-bit by 8-bit multiply or divide in 2.5 μ s at 10 V
- Interfaces directly with CDP1802
- Single supply voltage, 3-12 V
- Cascadable up to 4 units for 32-bit by 32-bit = 64-bit operation
- May be used as an I/O or memory device
- Full temperature range (-55 to +125°C)

* Available fourth quarter 1978.

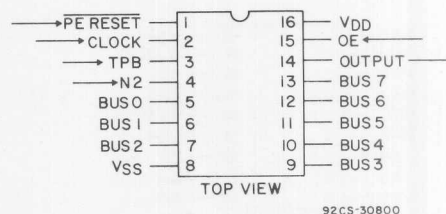
New Color Generator CDP1862 *



- NTSC compatible
- RGB compatible
- Optional on-chip Xtal-controlled oscillator
- Designed for use with the CDP1802 microprocessor and the CDP1861 TV Video Interface
- Low power
- Generates six colors plus black and white

* Available fourth quarter 1978.

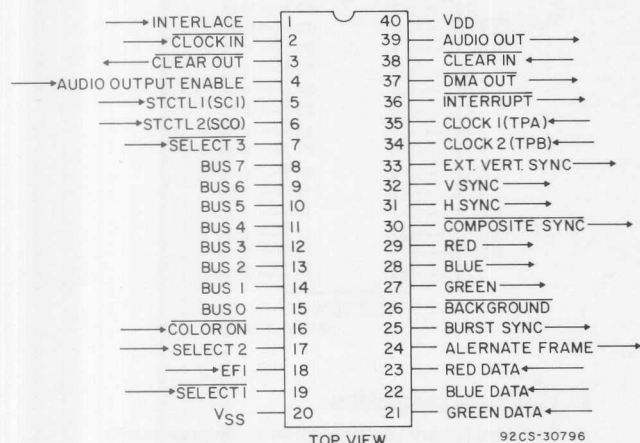
New Programmable Tone Generator CDP1863 *



- 256 possible frequencies in the audio range
- Designed for use with the CDP1802 microprocessor
- Frequency divide rate is set by program

* Available fourth quarter 1978.

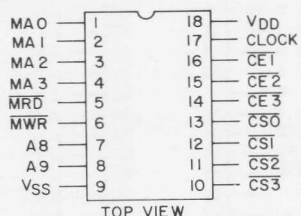
New PAL-Compatible TV Interface CDP1864 *



- RGB color
- Horizontal and vertical sync generation
- Interlaced or non-interlaced
- 1.75 MHz crystal operation
- Programmable mapped foreground color
- Four background colors under program control
- Single supply voltage
- Static CMOS technology
- Resolution of 192 vertical lines and 64 horizontal lines
- Interfaces directly with the CDP1802 microprocessor
- Supports bit-mapped video display for graphic flexibility
- Schmitt Trigger clear input and post-Schmitt Trigger clear output for power-on reset
- Programmable frequency divide for audio generation with output enable and default frequency

* Available fourth quarter 1978.

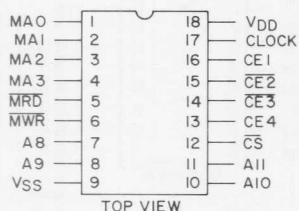
New Latch and Decoder Memory Interface CDP1866 *



- Low-power static CMOS technology
- Performs memory address latch and decoder functions
- Interfaces directly with multiplexed or non-multiplexed memory address buses
- Single-supply voltage, $V_{DD} = 4.5$ to 10.5 V
- Allows decoding for systems larger than 4096-words by 8-bits
- Intended for use with 1024-word by 4-bit RAMs

* Available fourth quarter 1978.

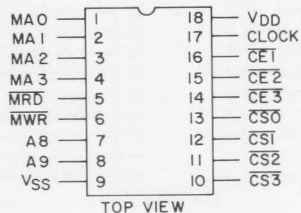
New Latch and Decoder Memory Interface CDP1867 *



- Low-power static CMOS technology
- Performs memory address latch and decoder functions
- Interfaces directly with multiplexed or non-multiplexed memory address buses
- Single-supply voltage, $V_{DD} = 4.5$ to 10.5 V
- Allows decoding for systems larger than 4096-words by 8-bits
- Intended for use with 4096-word by 1-bit RAMs

* Available fourth quarter 1978.

New Latch and Decoder Memory Interface CDP1868 *

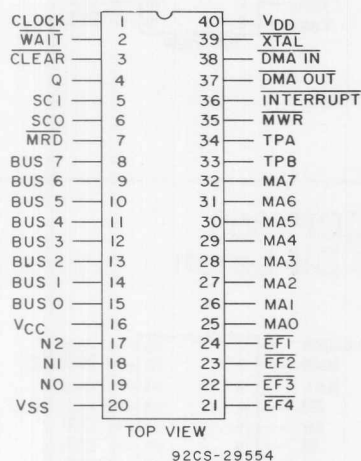


- Low-power static CMOS technology
- Performs memory address latch and decoder functions
- Interfaces directly with multiplexed or non-multiplexed memory address buses
- Single-supply voltage, $V_{DD} = 4.5$ to 10.5 V
- Intended for use with 1024-word by 4-bit RAMs
- Allows decoding for systems larger than 4096-words by 8-bits

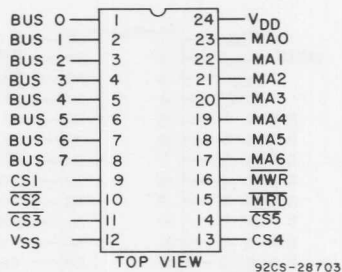
* Available fourth quarter 1978.

Terminal Assignment Diagrams

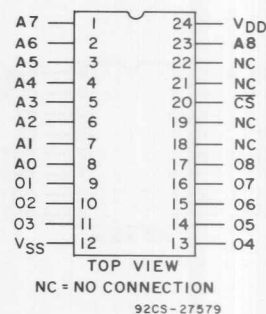
CDP1802 COSMAC Microprocessor



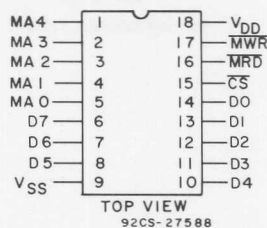
CDP1823 128 x 8 RAM



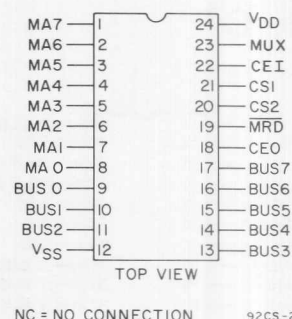
CDP1832 512 x 8 ROM



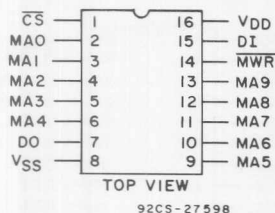
CDP1824 32 x 8 RAM



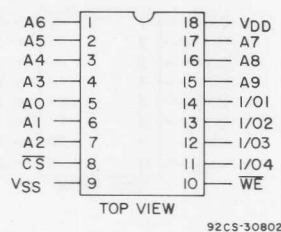
CDP1833 1024 x 8 ROM



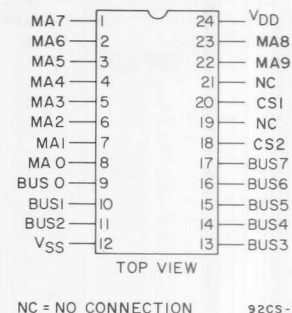
CDP1821 1024 x 1 RAM



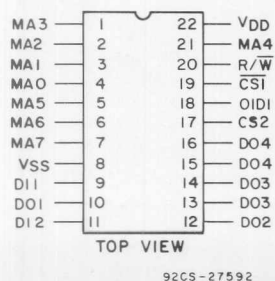
CDP1825 1024 x 4 RAM



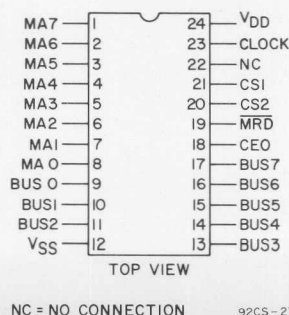
CDP1834 1024 x 8 ROM



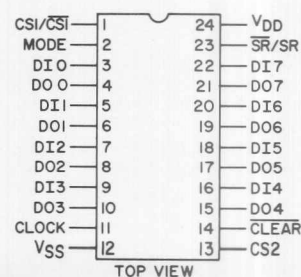
CDP1822 256 x 4 RAM



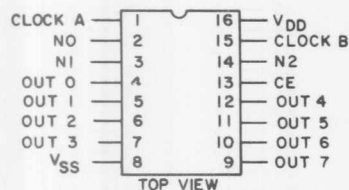
CDP1831 512 x 8 ROM



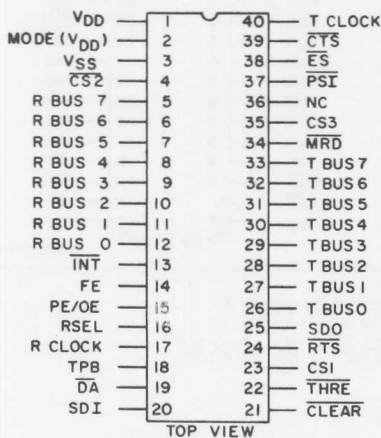
CDP1852 Byte I/O



CDP1853 N-Bit Decoder

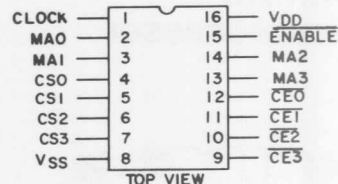


CDP1854 UART Mode 1

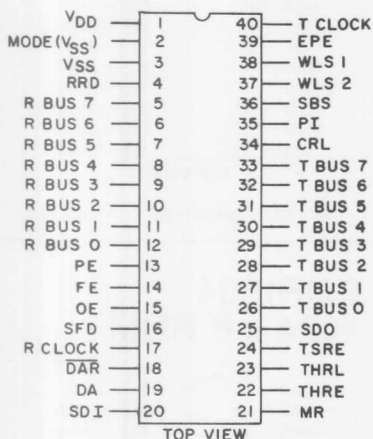


NC=NO CONNECTION

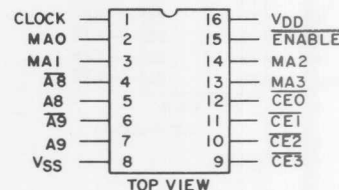
CDP1858 4-Bit Latch



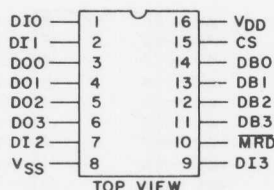
CDP1854 UART Mode 0



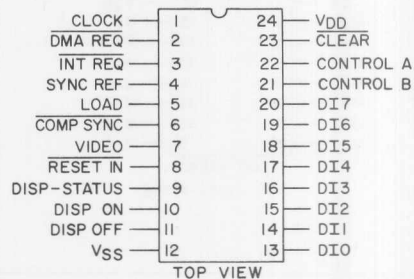
CDP1859 4-Bit Latch



CDP1856 Bus Buffer (Memory)



CDP1861 Video Display Controller

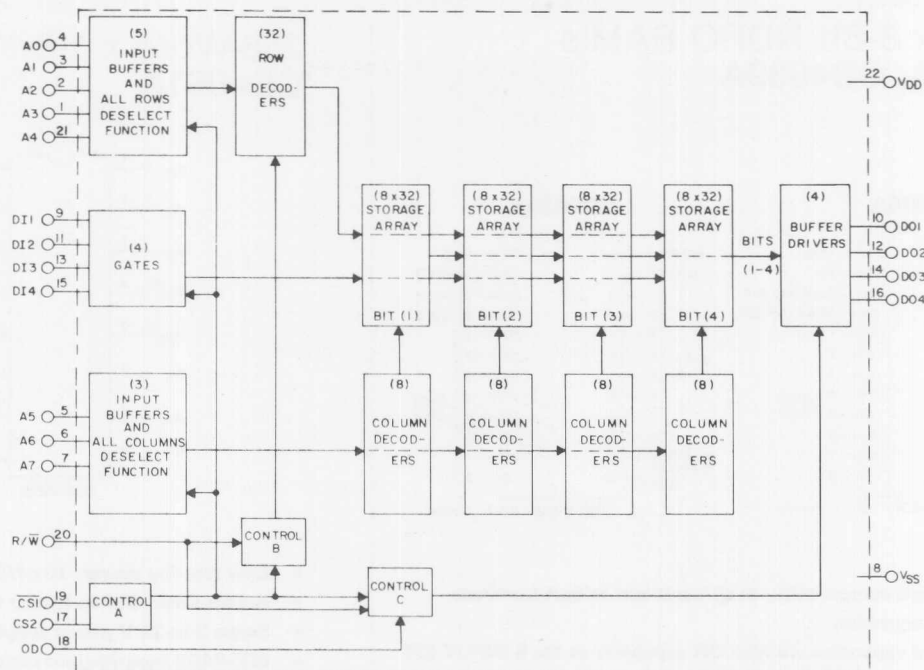


92CS-29730

MWS5000-Series Memory Products

256 x 4 RAM

MWS5101



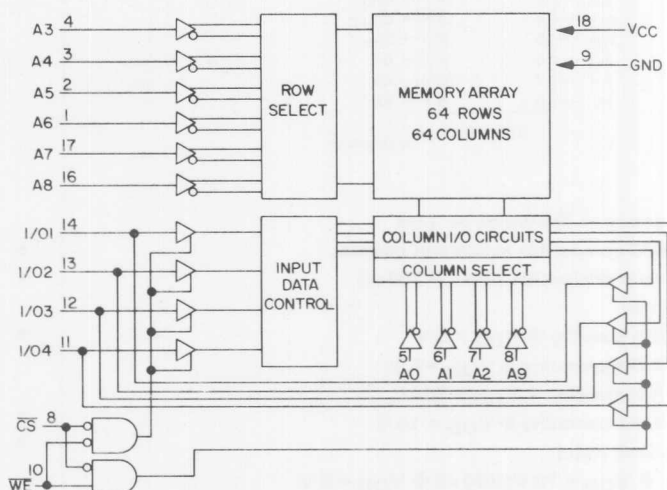
- Very low operating current — 4 mA typ. at $V_{DD} = 5$ V and cycle time = 1 μ s
- Industry standard pinout
- Two Chip-Select inputs — simple memory expansion
- Memory retention for standby battery voltage of 2 V min.
- Single-power-supply operation — 4 to 6.5 V

- High noise immunity — 30% of V_{DD} over the range 5 to 6.5 V
- TTL compatible
 - Drives one TTL load
 - Accepts TTL level inputs using pull-up resistor
- Output-Disable for common I/O systems
- 3-State data output for bus-oriented systems
- Separate data inputs and outputs

1024 x 4 RAM

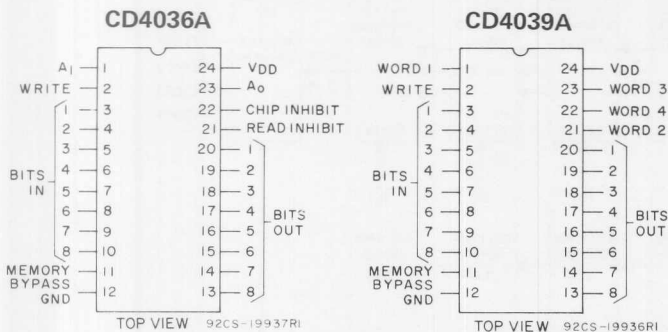
MWS5114

- Fully static operation
- 3-state outputs
- Industry standard 18-pin package
- Single power-supply operation: 4 to 6.5 V
- Common data input and output
- Memory retention for standby-battery voltage of 2 V min.
- All inputs and outputs are TTL compatible
- Low operating current



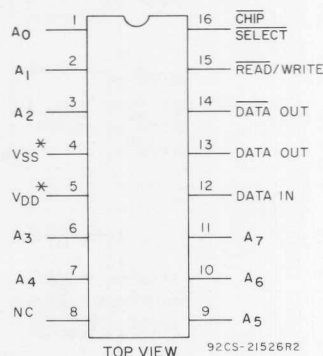
COS/MOS CD4000-Series Memory Products

4-Word x 8-Bit NDRO RAM's CD4036A, CD4039A



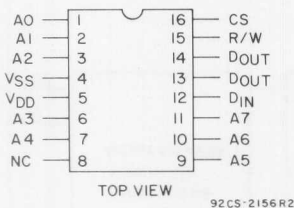
- COS/MOS logic compatibility at all input and output terminals
- Memory bit expansion
- Memory word expansion via Wire-OR capability at the 8 INPUT-BIT and 8 OUTPUT-BIT lines
- Memory bypass capability for all bits
- Buffering on all outputs
- CD4036A- on-chip binary address decoding, separate READ INHIBIT and WRITE controls
- Access Time — 200 ns (typ.) at $V_{DD} = 10\text{ V}$
- CD4039A-Direct word-line addressing

256-Word x 1-Bit Static RAM CD4061A



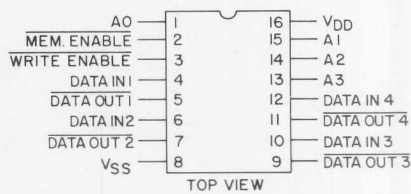
- Low standby power: 10 nW/bit (typ.) @ $V_{DD} = 10\text{ V}$
- Access time: 380 ns (max.) @ $V_{DD} = 10\text{ V}$
- Single 3-to-15 V power supply
- COS/MOS input/output logic compatibility
- TTL output drive capability
- Three-state data outputs for bus-oriented systems
- 1101-type pin designations
- Separate data output and data input lines
- Noise immunity: 45% of V_{DD} (typ.)
- Fully decoded addressing
- Single write/read control line

256-Word x 1-Bit Static RAM CD40061A



- Organization — 256-words by 1-bit
- COS/MOS compatible inputs and outputs
- Low power dissipation (typ.) @ 700 ns cycle time:
10 nW/Bit standby @ $V_{DD} = 5\text{ V}$
0.1 mW/Bit operating @ $V_{DD} = 5\text{ V}$
40 nW/Bit standby @ $V_{DD} = 10\text{ V}$
0.4 mW/Bit operating @ $V_{DD} = 10\text{ V}$
- Access time (typ.):
265 ns @ $V_{DD} = 10\text{ V}$; 700 ns @ $V_{DD} = 5\text{ V}$
- Noise immunity (typ.): 30% of V_{DD}
- TTL output drive capability
- 3-State complementary data outputs
- Separate data-in and data-out lines

16-Word x 4-Bit RAM CD40114B



- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
1 V at $V_{DD} = 5\text{ V}$ 2 V at $V_{DD} = 10\text{ V}$
2.5 V at $V_{DD} = 15\text{ V}$
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Input address register
- Low power consumption: 100 nW (typ.) at $V_{DD} = 5\text{ V}$
- Fast access time — 130 ns (typ.) at $V_{DD} = 10\text{ V}$
- 3-state outputs

Cross-Reference Guide

Note: RCA functionally equivalent type may not be identical with other manufacturer's type in every detail. Refer to published data for further information.

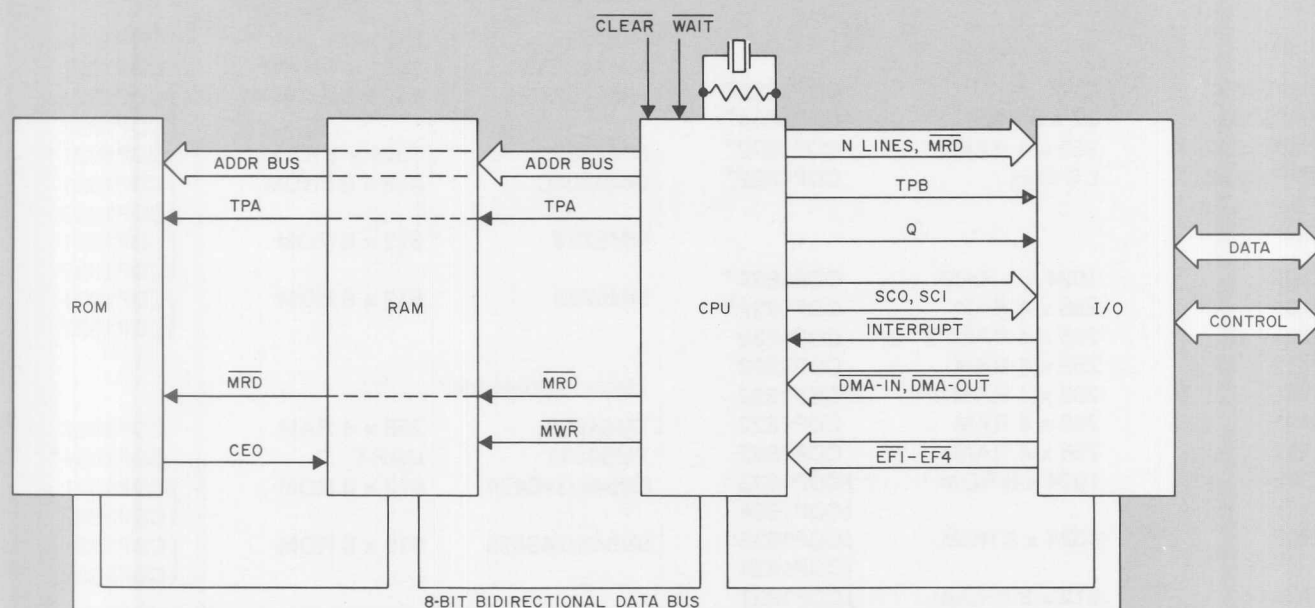
Type	Description	RCA Functionally Equivalent Type	Type	Description	RCA Functionally Equivalent Type
AMI			8708	1024 x 8 PROM	{ CDP1833 CDP1834*
S4025	1024 x 1 RAM	CDP1821	8212	Byte I/O	CDP1852
S6508	1024 x 1 RAM	CDP1821	3212	Byte I/O	CDP1852
S5101	256 x 4 RAM	CDP1822 *			
S6810-1	128 x 8 RAM	CDP1823	Intersil		
S3514	512 x 8 ROM	{ CDP1831 CDP1832	IM6508	1024 x 1 RAM	CDP1821
S6830	1024 x 8 ROM	{ CDP1833 CDP1834	IM6551	256 x 4 RAM	CDP1822
S1883	UART	CDP1854	IM6402/6403	UART	CDP1854*
Fairchild			Mostek		
MK3514	512 x 8 ROM	{ CDP1831 CDP1832	MK4009-9	1024 x 1 RAM	CDP1821
MK386k	I/O	CDP1852	MK4102P-1	1024 x 1 RAM	CDP1821 *
MK35342	1024 x 1 RAM	CDP1821	MK4102N-1	1024 x 1 RAM	CDP1821 *
MK35345	1024 x 1 RAM	CDP1821	MK2500P	512 x 8 ROM	{ CDP1831 CDP1832
MK93415	1024 x 1 RAM	CDP1821	MK2600P	512 x 8 ROM	{ CDP1831 CDP1832
MK93425	1024 x 1 RAM	CDP1821			
General Instruments			Motorola		
RA-3-4256	256 x 4 RAM	CDP1822	MCM2102	1024 x 1 RAM	CDP1821 *
RO-3-4096	512 x 8 ROM	{ CDP1831 CDP1832	MCM6810A	128 x 8 RAM	CDP1823
AY-3-1013			MCM6830	1024 x 8 ROM	{ CDP1833 CDP1834
AY-3-1014	UART	CDP1854*	MCM65308		
AY-3-1015			MCM68308		
Hughes			National		
HMPS1802	CPU	CDP1802*	INSB212	I/O	CDP1852
HMPS1824	32 x 8 RAM	CDP1824*	MM74C930	1024 x 1 RAM	CDP1821
HMPS1822	256 x 4 RAM	CDP1822*	MM87S295/6	512 x 8 EAROM	{ CDP1831 CDP1832
HMPS1852	I/O Port	CDP1852*	MM2102	1024 x 1 RAM	CDP1821 *
Intel			MM5204C	512 x 8 PROM	{ CDP1831 CDP1832
2102	1024 x 1 RAM	CDP1821*	MM5232	512 x 8 ROM	{ CDP1831 CDP1832
2101	256 x 4 RAM	CDP1822*	MM5233	512 x 8 ROM	{ CDP1831 CDP1832
2111	256 x 4 RAM	CDP1822			
2112	256 x 4 RAM	CDP1822	Texas Instruments		
4101	256 x 4 RAM	CDP1822	TMS4039	256 x 4 RAM	CDP1822
5101	256 x 4 RAM	CDP1822	TMS6011	UART	CDP1854*
8101	256 x 4 RAM	CDP1822	SN54S/74S474	512 x 8 ROM	{ CDP1831 CDP1832
2308	1024 x 8 ROM	{ CDP1833 CDP1834	SN54S/74S475	512 x 8 ROM	{ CDP1831 CDP1832
8308	1024 x 8 ROM	{ CDP1833 CDP1834			
2704	512 x 8 PROM	{ CDP1831 CDP1832*	Western Digital		
2708	1024 x 8 PROM	{ CDP1833 CDP1834	TR1602A	UART	CDP1854*

*Pin-for-pin compatible.

Complete 1800-Series microcomputer systems often use additional RCA solid state devices and other components

- COS/MOS Digital Integrated Circuits
- Linear Integrated Circuits
- Clocking
- Power Supplies

Typical CDP1802 microprocessor system



COS/MOS Integrated Circuits

Circuit	Function	Application	Circuit	Function	Application
CD4016 } CD4066 }	Transmission gates	Interfacing non-3-state output devices to the data bus	CD4520 } CD4060 }	Timers/counters	External time-keeping or sequence counting
CD4049 } CD4050 } CD40109 }	Level shifters	Interfacing components of various voltage levels	CD40105	FIFO	Interfacing systems with different clock rates
CD4041 } CD4050 } CD4049 } CD4502 }	Bus drivers	Bus driving into large loading	CD40101	Parity generation decoder	Parity generation and detection
CD4028 } CD4514 } CD4515 } CD4555 } CD4556 }	Decoders	Memory address or N-bit lines	CD4034 } CD4042 } CD4076 } CD4508 }	Data latches	Byte output devices
CD4056 } CD4511 }	Display devices	Interfacing data bus to display devices	CD4014 } CD4015 } CD4017 } CD4021 } CD4034 } CD4094 } CD40104 } CD40194 }	Shift registers	Serial I/O

Linear Integrated Circuits

Circuit	Function	Application	Circuit	Function	Application
CA3161E	BCD-to-7 Segment decoder/driver	Display	CA3094	Programmable power switch/amplifier	General-purpose control operations, timing
CA3724 } CA3725 }	1-A n-p-n transistor arrays	Relays, lamps, solenoid drivers	CA3098	Programmable Schmitt trigger with memory	Control applications, time delays, Schmitt trigger switching
CA3081 } CA3082 } CA3083 }	100-mA n-p-n transistor arrays	Drivers, interfacing	CA3600	COS/MOS transistor array	Linear operation
CA3130 } CA3140 }	BiMOS op-amps	High- Z_{IN} amplifiers and comparators, signal amplification, sensing	CA139 } CA239 } CA339 }	Quad voltage comparators	Multi-comparator applications
CA3085	Positive voltage regulator	On-board supply regulation	CA124 } CA224 } CA324 }	Quad op-amps	Multi-amplifier applications
CA3078	Micropower op-amp	Low-voltage applications	CA555	Timer	Precision timing and oscillator applications
CA3080	Variable-gain op-amp	Voltage comparator sample-and-hold, gain control, multiplex			

Clocking

Clock signal generation for the CDP1802 COSMAC microprocessor is simple and straightforward. The CDP1802 features of static operation and a single-phase clock make practical the use of the on-chip oscillator as the clock generator. The design of external oscillators, crystal or RC controlled, is also straightforward since they require only minimal circuitry. Recommended RC-controlled oscillator circuits include:

1. Inverter-type oscillators
2. RC oscillator using COS/MOS IC type CD4047A
3. Schmitt-trigger type RC oscillator

Any A-T cut crystal oscillator may be used as long as the crystal frequency is less than or equal to the maximum operating frequency specified in the CDP1802 data sheet. For improved stability, a parallel load capacitance of 20 to 24 pF can be used.

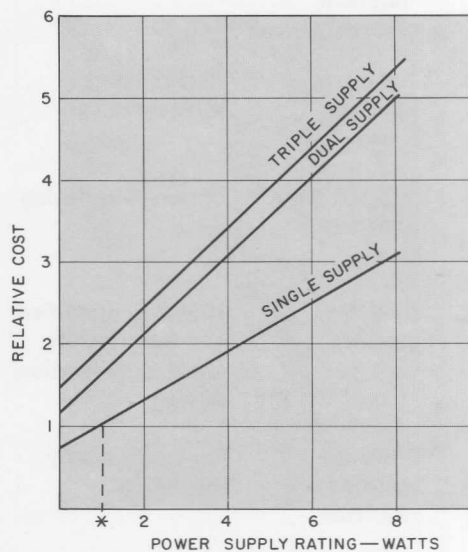
Possible crystal suppliers include:

Bliley Electronic Co.
Erie Technological Products
CTS Knights

Power Supplies

The cost of a power supply for use with CDP1800 Series microcomputer systems is minimized because of the advantages of the CMOS technology. The wide-operating-voltage range of 4.75 to 10.5 volts and the single power-supply requirement make CDP1802-based systems design simple and straightforward.

In fact, only a CMOS microprocessor like the CDP1802 is suitable for portable and battery back-up applications. Microprocessor systems incorporating the CDP1802, CDP1832, CDP1824, and CDP1852 have a typical power dissipation of only 100 mW. This small power requirement minimizes power-supply costs and helps to make COSMAC systems the first and best choice in microprocessor design.



* TYPICAL POWER SUPPLY REQUIREMENTS FOR COSMAC BASED SYSTEM.

Support Systems for the CDP1802 COSMAC microprocessor include an extensive line of hardware, software, and supplemental literature.

Features

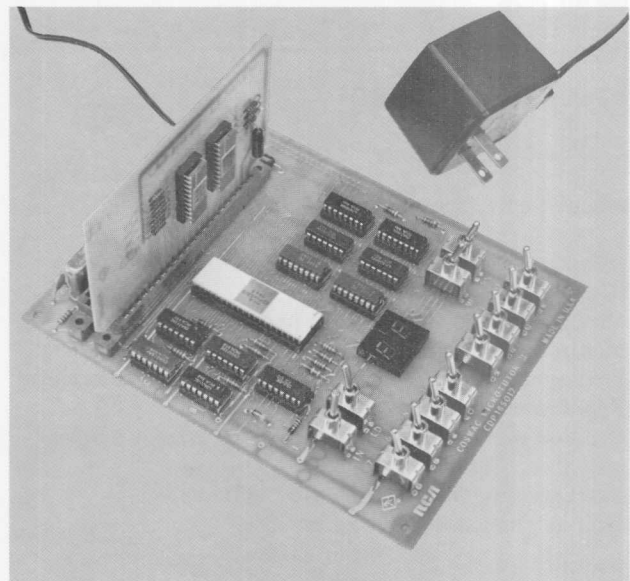
- Full spectrum of design aids: software, hardware, support, and literature
- Low cost systems for complete system design and debugging functions
- Hardware and software application support at your fingertips
- Offers "graduated steps" to microprocessor design
- Complete series of necessary literature and application notes

CDP18S012	COSMAC Microtutor II
CDP18S005	COSMAC Development System II
CDP18S805V1	Floppy Disk System
CDP18S020	COSMAC Evaluation Kit
CDP18S021	COSMAC Microterminal
CDP18S023	Power Supply
CDP18S024	EK/Assembler-Editor kit
CDP18S030	COSMAC Micromonitor
CDP18S031	Micromonitor Operating System (MOPS)
CDP18S826	Fixed Point Arithmetic Package
CDP18S827	Floating-Point Arithmetic Package
CDP18S91X	CSDP Timesharing Software

COSMAC Microtutor II CDP18S012

*To learn about programming
and microprocessors*

- Fully assembled unit
- Easy to use for quick hands-on microprocessor experience
- Expansion socket for additional user requirements
- Two-digit hexadecimal display
- Complete with power supply and 256 bytes of RAM
- Dimensions: 7" X 5.5"
- Manual: MPM-209
- Product Description: PD9



COSMAC Development System II

CDP18S005

For complete hardware and software system development

- Resident assembler and editor included for programming ease (paper tape and cassette)
- Fully assembled development system
- Terminal interface connections for 20 mA loop, RS232C, and Microterminal
- Accessable, socketed CDP1802 for simple interfacing to Micromonitor (CDP18S030)
- Interfaces directly to Floppy Disk System (CDP18S805)
- 4K-byte RAM included (expandable)
- Plug-in sockets for I/O expansion
- Plug-in sockets for memory expansion
- Over-all Dimensions: Length: 19-3/8"
Width: 12-3/4"
Height: 5-3/4"
- Manual: MPM-216
- Product Description: PD16



Accessories

To complement your COSMAC microprocessor system development tools

CDP18S102†	CDP1802 CPU Card
CDP18S103†	Control Card
CDP18S205V1†	4K RAM Card
CDP18S206†	Address Latch and Bank Select Card
CDP18S401†	ROM/RAM Card
CDP18S502†	Extender Card
*CDP18S402	PROM Programmer Card

CDP18S507†	Terminal Interface Card
CDP18S508	UART Interface Card
CDP18S509†	I/O Decode Card
CDP18S510	Byte I/O Card
**CDP18S801V1	Floppy Disk Drive
**CDP18S813	CDS II — Disk Interface Card
**CDP18S825	System Software (Disk)
CDP18S829	Blank Diskette

†Included with CDP18S005 (CDS II)

*Included with PROM Programmer CDP18S480

**Included with Floppy Disk System CDP18S805

Floppy Disk System

CDP18S805V1

For high-speed program development

- Interfaces directly to COSMAC Development System (CDP18S005)
- Dual disk drive mechanism provides 1/2 M bytes on line
- Monitor and disk control programs in firmware
- Programmed system diskette and blank diskette supplied
- Rapid assembly and edit capability
- Disk-to-tape, disk diagnostic, memory save, and other utility software also supplied
- Extra blank diskettes available (CDP18S829)
- Over-all Dimensions: Length: 20 3/4"
Width: 19 1/4"
Height: 7 1/4"
- Manual: MPM-217
- Product Description: PD17



Note: Alternate model for 220-V, 50-Hz operation also available: CDP18S805V2

PROM Programmer CDP18S480

For use with the CDS-II

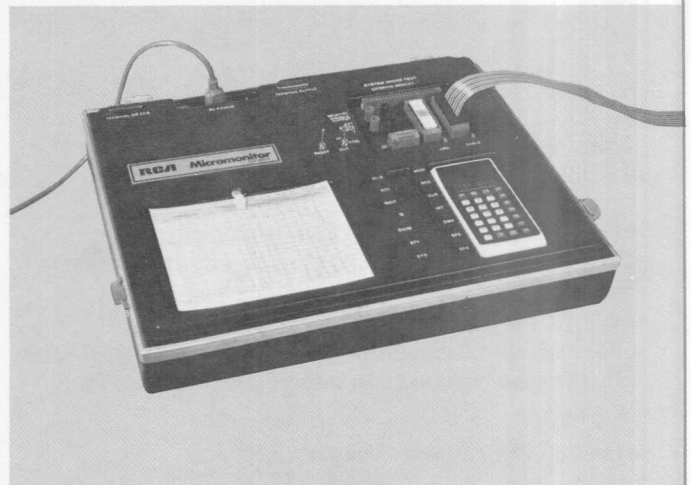
- Programs Intel 2704, 2708, 2716, 2758, and equivalent PROM's
- Can read Intel 1702-type PROM's
- Three versions:
 - CDP18S480 — Disk
 - CDP18S480V1 — Paper Tape
 - CDP18S480V2 — Cassette
- Includes CDP18S402 PROM Programmer Card and versatile operating program
- Program is supplied in both source and assembly language
- Over-all Dimensions: 4.5" X 7.5"



COSMAC Micromonitor CDP18S030

For in-circuit real-time hardware and software debugging.

- Stand-alone unit
- Single connection to any CDP1802 system
- 45 separate debug commands
- For field servicing, production testing, or debugging prototypes
- Minimal effects on system under test—actually uses the system's processor instead of "emulating" it
- Operates from built-in keyboard and display or interfaces external terminal for hard copy—20 mA, RS232C; 110, 300, and 1200 baud
- Data-logs several CPU registers at user determined points
- Self-contained, portable unit weighs only 16 lbs
- Capable of bidirectional disk-to-system transfers of data and commands when operated with MOPS option CDP18S831
- Built-in tracking power supply
- Over-all dimensions: Length: 18½"
Width: 14½"
Height: 6"
- Manual: MPM-218
- Product Description: PD18



COSMAC Evaluation Kit CDP18S020

EK/Assembler-Editor Kit CDP18S024

Complete system for machine-language programming and prototyping

- Low-cost prototyping and evaluation system for the COSMAC family
- Serial interfacing capability to 20 mA loop or RS232 terminals
- Microterminal option available (CDP18S021)
- 256 bytes of RAM included in 18S020
- 4-K bytes of RAM included in 18S024
- Large separate area for user circuitry
- Single-step capability
- Resident Editor and Assembler Tape programs supplied with CDP18S024
- Memory Address, Data, State Code, Q-Line, Clear, Wait signals all monitored and displayed on LEDs
- Over-all Dimensions: 14" X 9.7"
User I/O Area: 7" X 4 "
- Manual: MPM-224
- Product Description: PD24



COSMAC Microterminal CDP18S021

Low-cost alternative for TTY, CRT, or other terminals in 1802-based system

- Fully assembled, portable, self-contained terminal
- Terminal and control ROM plug directly into Evaluation Kit and CDS
- 8-digit, 7-segment, LED hexadecimal display
- Features simultaneous memory address and data display
- Display can be used as an output under user software control
- Over-all Dimensions: Length: 5.5"
Width: 3"
Height: 0.7"
- Manual: MPM-212
- Product Description: PD12

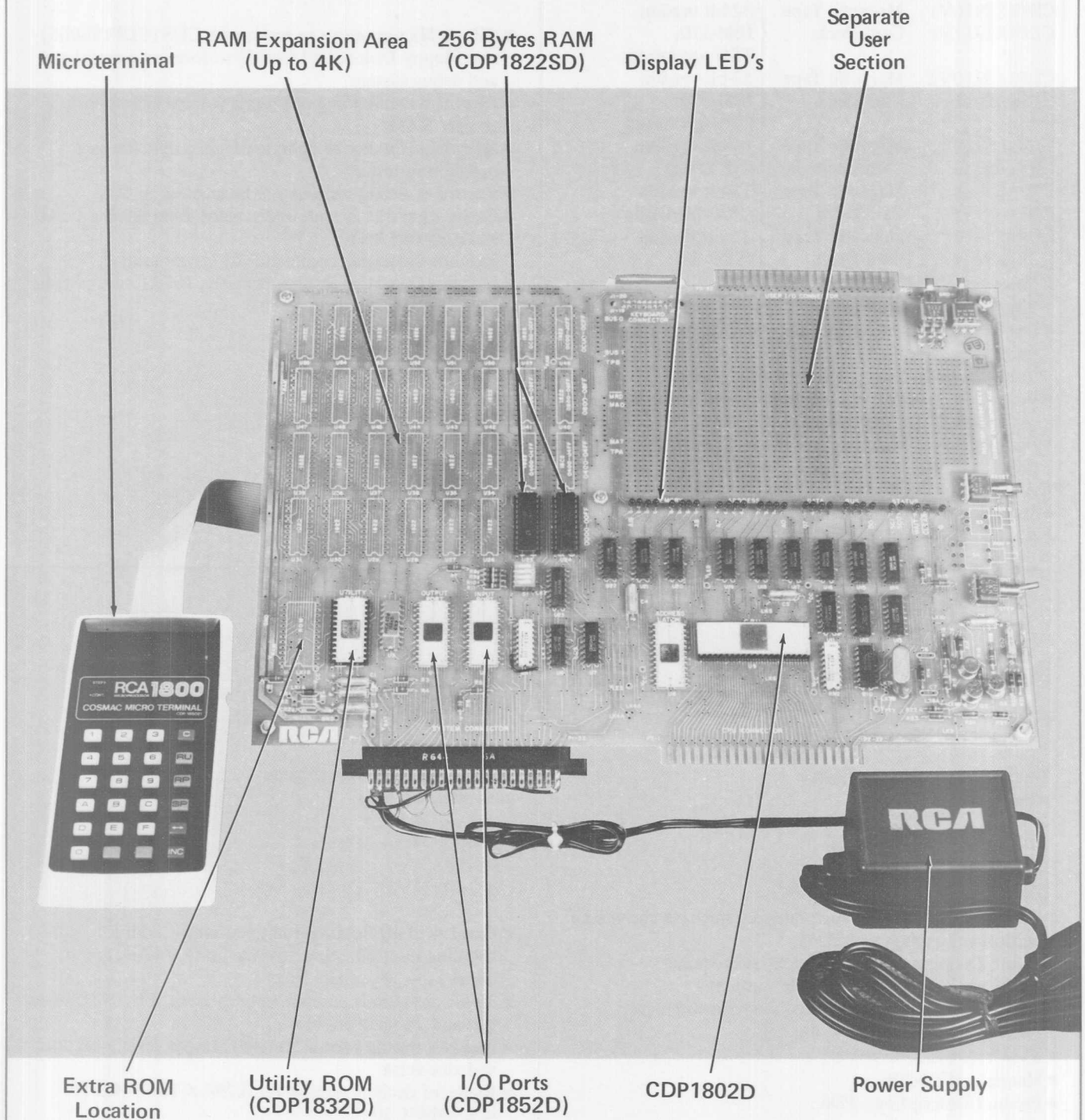
Power Supply CDP18S023

Lightweight, inexpensive system power supply

- Suitable for 5 V power supply for Evaluation Kit CDP18S020 and Microterminal
- Plugs into any standard wall outlet
- Ratings:
Input — 110V, 50-60 Hz, 9W
Output — 5VDC, 600 mA
- Over-all Dimensions: Length: 3.5"
Width: 1.75"
Height: 2"

CDP18S025

Evaluation Kit, Microterminal, and Power Supply



COSMAC Software Development Package (CSDP)

For non-resident program development

CDP18S910V1	Magnetic Tape	{ 32-bit version IBM-370, TSO optimized
CDP18S911V1	Card Deck	
CDP18S910V2	Magnetic Tape	{ 32-bit version IBM-370, CMS optimized
CDP18S911V2	Card Deck	
CDP18S912	Magnetic Tape	{ 16-bit version (HP-2100)
CDP18S913	Card Deck	
CDP18S914	Magnetic Tape	{ 16-bit version (PDP-11, DOS)
CDP18S915	Card Deck	
CDP18S916	Magnetic Tape	{ 32-bit version (PDP-10)
CDP18S917	Card Deck	

- Cross-assembler, simulator, and debugger
- Written in portable Fortran IV
- One-pass assembler with classical and extended assembly language power
- Versatile, powerful, and easy to use commands
- Interactive simulator/debugger acts as a "software oscilloscope" for multiple debug features
- Directly downloads programs into COSMAC Development System
- Available on commercial timesharing networks
- Manuals: MPM-202 and MPM-204
- Product Description: PD2

Micromonitor Operating System (MOPS) CDP18S831

*Optional package for operating
Micromonitor with disk files*

- Allows Micromonitor to work with CDS (CDP18S005) and Floppy Disk (CDP18S805) to form a powerful test and debug system
- Permits down-loading of programs from floppy disk to user RAM
- Micromonitor can be operated from a disk file as a production tester
- Record of debug sessions can be created on disk
- Entire state of a system under test can be saved on disk and reloaded later
- Extends debugging commands of Micromonitor
- Includes Operating System diskette, UART card plug-in for CDS, and connecting cable
- Manual: MPM-231
- Product Description: PD31

Binary Fixed-Point Arithmetic Subroutines

*To ease programming of often
used routines*

CDP18S826	Diskette
CDP18S826V1	Paper Tape
CDP18S826V2	Cassette Tape

- Consists of 31 routines including register save and mathematical companion operations
- 16-bit 2's-complement arithmetic subroutines
- Easily used multiply and divide routines
- Features double precision capability for the basic functions of (+), (-), (X), and ($\div$)
- BCD $\rightleftharpoons$ binary conversion
- Manual: MPM-206
- Product Description: PD6

Binary Floating-Point Arithmetic Subroutines

*To ease programming of often
used routines*

CDP18S827	Diskette
CDP18S827V1	Paper Tape
CDP18S827V2	Cassette Tape

- Consists of 10 floating-point routines — addition, subtraction, multiplication, division, sine, cosine, arctan, natural log, e^x , square root
- 32-bit operations on numbers represented by 8 exponent bits and 24 mantissa bits
- Includes routines for BCD-to-floating-point conversion and vice versa
- Range of decimal numbers is $0.294 \times 10^{-38} \leq \text{FPN} \leq 1.7014 \times 10^{38}$
- Manual: MPM-207
- Product Description: PD7

Literature Order Form

Production Description #		Price*	Qty.	Total
PD1	Price List and Literature Order Form	FREE**		
PD2	COSMAC Software Development Package (CSDP)	\$ 0.10	_____	_____
PD6	Fixed Point Binary Arithmetic Subroutines	0.10	_____	_____
PD7	Floating-Point Arithmetic Subroutine Diskette CDP18S827	0.10	_____	_____
PD9	Microtutor II	0.10	_____	_____
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PD16	COSMAC Developmental System II	0.10	_____	_____
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PD31	Micromonitor Operating System CDP18S831	0.10	_____	_____
Manuals				
MPM-201	User Manual for the CDP1802 COSMAC Microprocessor	5.00	_____	_____
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MPM-203	Evaluation Kit Manual for the CDP1802 COSMAC Microprocessor	15.00	_____	_____
MPM-204	Installation Manual for COSMAC Software Development Package	10.00	_____	_____
MPM-206	Binary Arithmetic Subroutines for the COSMAC Microprocessor	5.00	_____	_____
MPM-207	Floating Point Binary Arithmetic Subroutines	2.00	_____	_____
MPM-209	COSMAC Microtutor Manual	2.00	_____	_____
MPM-212	COSMAC Instruction Manual for COSMAC Microterminal	2.00	_____	_____
MPM-216	Operator Manual for the COSMAC Developmental System II CDP18S005	10.00	_____	_____
MPM-217	Floppy Disk System II CDP18S805 Instruction Manual	10.00	_____	_____
MPM-218	Instruction Manual for the RCA COSMAC Micromonitor CDP18S030	5.00	_____	_____
MPM-224	EK/Assembler-Editor Manual	15.00	_____	_____
MPM-231	Micromonitor Operating System (MOPS) CDP18S831 Users' Guide	2.00	_____	_____
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Other		Price*	Qty.	Total
MPG-180	Product Guide	0.50	_____	_____
DL	Distributor List	FREE	_____	_____
MPM-920	Instruction Summary for the CDP1802 COSMAC Microprocessors	0.10	_____	_____
PD30	ROM Purchase Policy and Data Programming Instructions	0.10	_____	_____
Data Sheets	(Indicate type numbers) _____			

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COSMAC Register and Instruction Summary

Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer
N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high-order 4 bits)
IE	1 Bit	Interrupt Enable
Q	1 Bit	Output Flip-Flop

Instruction Set

The COSMAC instruction summary is given below. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W)

R(W).1: Higher-order byte of R(W)

Operation Notation

$M(R(N)) \rightarrow D; R(N) + 1$

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

Instruction Summary

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	$M(R(N)) \rightarrow D$; FOR N NOT 0
LOAD ADVANCE	LDA	4N	$M(R(N)) \rightarrow D; R(N) + 1$
LOAD VIA X	LDX	F0	$M(R(X)) \rightarrow D$
LOAD VIA X AND ADVANCE	LDXA	72	$M(R(X)) \rightarrow D; R(X) + 1$
LOAD IMMEDIATE	LDI	F8	$M(R(P)) \rightarrow D; R(P) + 1$
STORE VIA N	STR	5N	$D \rightarrow M(R(N))$
STORE VIA X AND DECREMENT	STXD	73	$D \rightarrow M(R(X)); R(X) - 1$
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	$R(N) + 1$
DECREMENT REG N	DEC	2N	$R(N) - 1$
INCREMENT REG X	IRX	60	$R(X) + 1$
GET LOW REG N	GLO	8N	$R(N).0 \rightarrow D$
PUT LOW REG N	PLO	AN	$D \rightarrow R(N).0$
GET HIGH REG N	GHI	9N	$R(N).1 \rightarrow D$
PUT HIGH REG N	PHI	BN	$D \rightarrow R(N).1$
LOGIC OPERATIONS**			
OR	OR	F1	$M(R(X)) \text{ OR } D \rightarrow D$
OR IMMEDIATE	ORI	F9	$M(R(P)) \text{ OR } D \rightarrow D; R(P) + 1$
EXCLUSIVE OR	XOR	F3	$M(R(X)) \text{ XOR } D \rightarrow D$
EXCLUSIVE OR IMMEDIATE	XRI	F8	$M(R(P)) \text{ XOR } D \rightarrow D; R(P) + 1$
AND	AND	F2	$M(R(X)) \text{ AND } D \rightarrow D$
AND IMMEDIATE	ANI	FA	$M(R(P)) \text{ AND } D \rightarrow D; R(P) + 1$
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, $LSB(D) \rightarrow DF$, $0 \rightarrow MSB(D)$
SHIFT RIGHT WITH CARRY	SHRC	76*	SHIFT D RIGHT, $LSB(D) \rightarrow DF$, $DF \rightarrow MSB(D)$
RING SHIFT RIGHT	RSHR		
SHIFT LEFT	SHL	FE	SHIFT D LEFT, $MSB(D) \rightarrow DF$, $0 \rightarrow LSB(D)$
SHIFT LEFT WITH CARRY	SHLC	7E*	SHIFT D LEFT, $MSB(D) \rightarrow DF$, $DF \rightarrow LSB(D)$
RING SHIFT LEFT	RSHL		

Instruction Summary (cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
ARITHMETIC OPERATIONS**			
ADD	ADD	F4	$M(R(X)) + D \rightarrow DF, D$
ADD IMMEDIATE	ADI	FC	$M(R(P)) + D \rightarrow DF, D; R(P) + 1$
ADD WITH CARRY	ADC	74	$M(R(X)) + D + DF \rightarrow DF, D$
ADD WITH CARRY, IMMEDIATE	ADCI	7C	$M(R(P)) + D + DF \rightarrow DF, D; R(P) + 1$
SUBTRACT D	SD	F5	$M(R(X)) - D \rightarrow DF, D$
SUBTRACT D IMMEDIATE	SDI	FD	$M(R(P)) - D \rightarrow DF, D; R(P) + 1$
SUBTRACT D WITH BORROW	SDB	75	$M(R(X)) - D - (NOT DF) \rightarrow DF, D$
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	$M(R(P)) - D - (NOT DF) \rightarrow DF, D; R(P) + 1$
SUBTRACT MEMORY	SM	F7	$D - M(R(X)) \rightarrow DF, D$
SUBTRACT MEMORY IMMEDIATE	SMI	FF	$D - M(R(P)) \rightarrow DF, D; R(P) + 1$
SUBTRACT MEMORY WITH BORROW	SMB	77	$D - M(R(X)) - (NOT DF) \rightarrow DF, D$
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	$D - M(R(P)) - (NOT DF) \rightarrow DF, D; R(P) + 1$
BRANCH INSTRUCTIONS—SHORT BRANCH			
SHORT BRANCH	BR	30	$M(R(P)) - R(P).0$
NO SHORT BRANCH (SEE SKP)	NBR	38*	$R(P) + 1$
SHORT BRANCH IF D=0	BZ	32	IF $D=0$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF D NOT 0	BNZ	3A	IF $D \text{ NOT } 0$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF DF=1	BDF	33*	IF $DF=1$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B*	IF $DF=0$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=1	BQ	31	IF $Q=1$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF Q=0	BNQ	39	IF $Q=0$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF1=1	B1	34	IF $EF1=1$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF1=0	BN1	3C	IF $EF1=0$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF2=1	B2	35	IF $EF2=1$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF2=0	BN2	3D	IF $EF2=0$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF3=1	B3	36	IF $EF3=1$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF3=0	BN3	3E	IF $EF3=0$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF4=1	B4	37	IF $EF4=1$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF4=0	BN4	3F	IF $EF4=0$, $M(R(P)) - R(P).0$ ELSE $R(P) + 1$
BRANCH INSTRUCTIONS—LONG BRANCH			
LONG BRANCH	LBR	C0	$M(R(P)) - R(P).1$ $M(R(P) + 1) - R(P).0$ $R(P) + 2$
NO LONG BRANCH (SEE LSKP)	NLBR	C8*	
LONG BRANCH IF D=0	LBZ	C2	IF $D=0$, $M(R(P)) - R(P).1$ $M(R(P) + 1) - R(P).0$ ELSE $R(P) + 2$
LONG BRANCH IF D NOT 0	LBNZ	CA	IF $D \text{ NOT } 0$, $M(R(P)) - R(P).1$ $M(R(P) + 1) - R(P).0$ ELSE $R(P) + 2$
LONG BRANCH IF DF=1	LBDF	C3	IF $DF=1$, $M(R(P)) - R(P).1$ $M(R(P) + 1) - R(P).0$ ELSE $R(P) + 2$
LONG BRANCH IF DF=0	LBNF	CB	IF $DF=0$, $M(R(P)) - R(P).1$ $M(R(P) + 1) - R(P).0$ ELSE $R(P) + 2$
LONG BRANCH IF Q=1	LBQ	C1	IF $Q=1$, $M(R(P)) - R(P).1$ $M(R(P) + 1) - R(P).0$ ELSE $R(P) + 2$
LONG BRANCH IF Q=0	LBNQ	C9	IF $Q=0$, $M(R(P)) - R(P).1$ $M(R(P) + 1) - R(P).0$ ELSE $R(P) + 2$

Instruction Summary (cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38*	R(P) + 1
LONG SKIP (SEE NLBR)	LSKP	C8*	R(P) + 2
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P) + 2 ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P) + 2 ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P) + 2 ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P) + 2 ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P) + 2 ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P) + 2 ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P) + 2 ELSE CONTINUE
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P←X; R(2)←1
RETURN	RET	70	M(R(X))→(X,P); R(X) + 1 1→IE
DISABLE*	DIS	71	M(R(X))→(X,P); R(X) + 1 0→IE
INPUT-OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS; R(X) + 1; N LINES = 1
OUTPUT 2	OUT 2	62	M(R(X))→BUS; R(X) + 1; N LINES = 2
OUTPUT 3	OUT 3	63	M(R(X))→BUS; R(X) + 1; N LINES = 3
OUTPUT 4	OUT 4	64	M(R(X))→BUS; R(X) + 1; N LINES = 4
OUTPUT 5	OUT 5	65	M(R(X))→BUS; R(X) + 1; N LINES = 5
OUTPUT 6	OUT 6	66	M(R(X))→BUS; R(X) + 1; N LINES = 6
OUTPUT 7	OUT 7	67	M(R(X))→BUS; R(X) + 1; N LINES = 7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS←D; N LINES = 1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS←D; N LINES = 2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS←D; N LINES = 3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS←D; N LINES = 4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS←D; N LINES = 5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS←D; N LINES = 6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS←D; N LINES = 7

* THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

♦ THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF.

AFTER AN ADD INSTRUCTION:

DF = 1 DENOTES A CARRY HAS OCCURRED

DF = 0 DENOTES A CARRY HAS NOT OCCURRED

AFTER A SUBTRACT INSTRUCTION:

DF = 1 DENOTES NO BORROW. D IS A TRUE POSITIVE NUMBER

DF = 0 DENOTES A BORROW. D IS TWO'S COMPLEMENT THE SYNTAX—(NOT DF) DENOTES THE SUBTRACTION OF THE BORROW

An idle instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request (INTERRUPT, DMA-IN, or DMA-OUT) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

1. Long-Branch, Long-Skip and No Op instructions are the only instructions that require three cycles to complete (1 fetch + 2 execute).

Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

The long-branch instructions can:

- Branch unconditionally
- Test for D=0 or D≠0
- Test for DF=0 or DF=1
- Test for Q=0 or Q=1
- Effect an unconditional no branch

If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch.

2. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

The short-branch instructions can:

- Branch unconditionally
- Test for D=0 or D≠0
- Test for DF=0 or DF=1
- Test for Q=0 or Q=1
- Test the status (1 or 0) of the four EF flags
- Effect an unconditional no branch

If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch with the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch.

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

They can:

- Skip unconditionally
- Test for D=0 or D≠0
- Test for DF=0 or DF=1
- Test for Q=0 or Q=1
- Test for IE=1

If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

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